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Ultralow-power Pipelined Adder Using Efficient Charge Recovery Logic

T. Srinivasa Rao[1], S. Sai Teja Sri[2], A.V.N.Tilak[3]

[1]*Department of Electronics & Communication Engineering, Gudlavalleru Engineering College, e-mail: srinivasthammisetti6@gmail.com, India.*

[2]*Department of Electronics & Communication Engineering, Gudlavalleru Engineering College, e-mail: sudani.tejasri@gmail.com, India.*

[3]*Department of Electronics & Communication Engineering, Gudlavalleru Engineering College, e-mail: avntilak@yahoo.com, India.*

Abstract - *Adders are important building blocks in many digital systems and the performance of these systems depends mainly on the speed of addition, power consumption and area occupied by the adder circuit. Portable and battery operated devices require very low power for their efficient operation. In this work a carry save adder is designed using pipelined architecture to improve the speed and implemented with efficient charge recovery logic (ECRL) for reducing the power dissipation. The simulations carried out using Mentor Graphics tool at 130 nm technology node indicate an improvement of 99.4% in speed with pipelining for the static CMOS 4-bit carry save adder. With ECRL logic the power dissipation is found to be lowered by 46.3% as compared to static CMOS pipelined adder.*

Key words: *Carry save adder, ECRL logic, pipelining, ultralow-power, delay*

I. Introduction

Due to increase in complexity of today's VLSI circuits, there is a significant increase in the power consumption. As the demand for portable battery operated devices is increasing rapidly, the design of power efficient circuits is gaining importance [1–2]. Adder is the important building block in many digital systems such as data path of the microprocessor, digital signal processor, cryptography, and memory addressing. In all these systems, the adder lies in the critical path that affects the overall performance of the system.

Depending upon the area, delay, and power consumption, the various adders are categorized as ripple carry adder, carry select adder, carry lookahead adder, and carry save adder among others [3-9]. Designing adders with fast addition operation and low power consumption along with low area is still a challenging issue.

In this work a carry save adder [10] is chosen as its latency is same as that of full adder. It is simply a parallel ensemble of n full-adders without any horizontal connection, and the carry is saved as an output and not propagated to the next higher-order adder. It reduces the addition of 3 numbers to the addition of 2 numbers. The propagation delay is independent of the number of bits, and the amount of circuitry is less than that of a carry select adder. In order to reduce the delay pipelining architecture [11-12] is chosen and efficient charge recovery logic (ECRL) [13-15] is used for lowering the power dissipation.

This paper is organized as follows: section II gives the background of pipelining concept and ECRL adiabatic logic is given in section III. Section IV shows the implementation of pipelined carry save adder using conventional CMOS and ECRL logic. Finally, results and conclusions are given in sections V and VI respectively.

II. Pipelining Concept

The increasing clock rates of the deep submicron technologies demand fast addition, whereas the parallel processing systems require adders with smaller area. In conventional n-stage adder all the stages are performed with single clock cycle. However, the frequency of this clock is restricted due to the circuit constraints. Hence, whenever the addition of large number of values is to be performed, the traditional adders proved to be inefficient. This latency could be overcome if the concept of pipelining is introduced in the simple adder. The adder is subdivided into stages, which were pipelined according to the proper timing sequences. The clock frequency of the pipelined adder could be higher than that used for traditional adder. Also, while the two inputs are being processed and passed on to subsequent stages, new inputs enter the initial stage and the cycle continues. This results in overall faster operation and hence throughput.

Pipelined adder design involves insertion of one register into each stage of the design, from input to output. Input data is fed continuously to the adder and

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the summation is achieved in pipelined adder in every clock cycle through the steps, comparing, swapping, shifting, addition, and normalization. Each pipeline stage performs operations independent of others.

Fig. 1 depicts an example of a pipelined circuit. It shows three nodes of a combinational circuit with registers inserted for each stage from input to output.

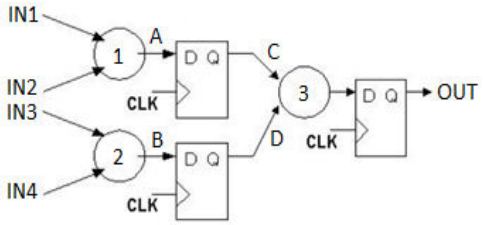

Fig. 1. Pipelined architecture

III. ECRL Logic

Efficient charge recovery logic (ECRL) is one of the adiabatic logic [16-18] families. Adiabatic is a reversible thermodynamic process that occurs without loss or gain of energy. Adiabatic logic uses power clock, unlike traditional power sources used by conventional CMOS logic circuits, to achieve efficient recycling of the charge stored in load capacitor. These circuits are characterized by minimum dynamic switching energy loss due to the energy recycling. The charging and discharging processes of adiabatic logic are shown in Fig. 2.

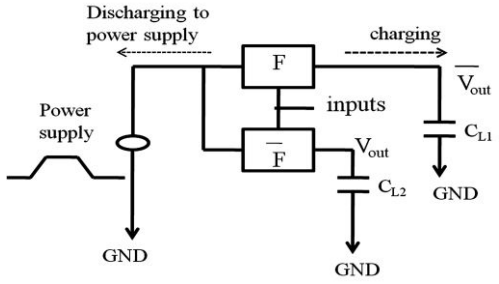

Fig. 2. Adiabatic charging and discharging

When the charge is supplied through a constant current source, the energy dissipated in an adiabatic circuit is given as

$$E_{diss} = \frac{RC}{T} C V_{dd}^2 \qquad (1)$$

Where R is the effective resistance of the driven device, C is the load capacitance, T is the charging/discharging time of the capacitor, and V_{dd} is the full swing of the power clock. If T>>2RC, the energy dissipated by the adiabatic circuit is less than the conventional CMOS circuit.

Various adiabatic logic families including positive feedback adiabatic logic (PFAL), ECRL, clocked adiabatic logic (CAL) and two-phase clocked CMOS adiabatic logic (2PC2AL) are reported in literature. As the power dissipation and complexity is minimum, ECRL logic is chosen in this work to implement the pipelined carry save adder. The ECRL buffer/inverter shown in Fig. 3 consists of two cross-coupled PMOS devices P1 and P2 to store the information and NMOS devices for implementing the logic. The PMOS transistors in both pre-charge and recover phases will give rise to full output swing. V_{pc} is the ac supply of ramp type with 3.3V peak amplitude and 1MHz frequency and IN and OUT are the input signals and outputs respectively.

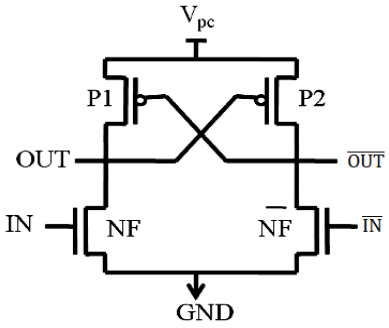

Fig. 3. ECRL buffer/ inverter

IV. Carry Save Adder

IV.I. Static CMOS Carry Save Adder

Schematic of a 4-bit carry save adder using static CMOS logic is shown in Fig. 4. In the figure, a0 – a3 and b0 – b3 are the inputs, S0 – S3 are the sum outputs, and C_{out} is the output carry.

In order to improve the throughput pipelining technique is applied for the carry save adder shown. Fig. 5 shows a 4-bit pipelined carry save adder. At each clock cycle a new input is applied to the circuit. Therefore, because of the registers, it takes three clock cycles to get the first result. Thus the circuit has a latency of three clock cycles. Then, after each clock cycle, a new result is obtained at the output. The throughput of this circuit is then one clock cycle plus $T_{co,}$ the time from one clock cycle to the output of a register.

The pipelined structure of N combinational logic blocks can be represented as shown in the Fig. 5. Each segment consists of an input latch followed by a combinational circuit. The input latch holds the input data and the combinational circuit performs its operation in the particular segment. The output of this segment is given as input to the input latch of the next segment. Common clock is applied to all the latches

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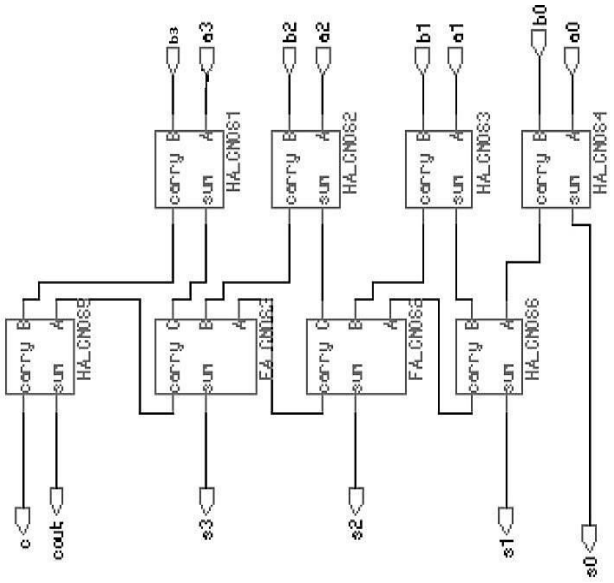

Fig. 4. 4-bit carry save adder using static CMOS logic

after enough time has elapsed to perform the sub-operations in all the segments.

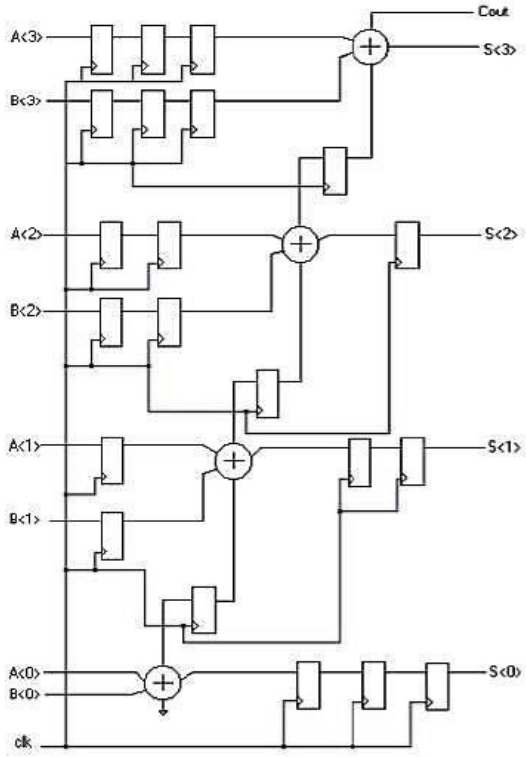

Fig. 5. 4-bit pipelined carry save adder using static CMOS logic

IV.II. 4-bit Pipelined Carry Save Adder using ECRL Logic

A 4-bit pipelined carry save adder using ECRL logic is synthesized from NAND, XOR gates, D-flip-flops, and full adders. Fig. 6 shows the schematic of an ECRL two-input AND/NAND gate.

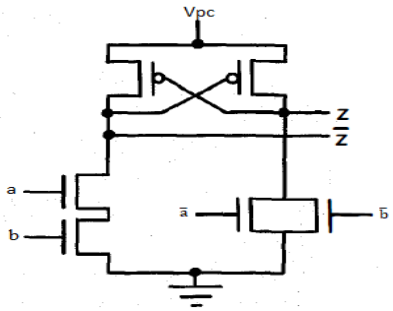

Fig. 6. ECRL AND/NAND gate

The two inputs are a and b. As shown in the figure, it consists of two cross-coupled PMOS transistors and NMOS transistors in the circuit. The output signal z is generated so that the power clock generator can always drive a constant load capacitance independent of the input signal.

The XOR/XNOR gate is implemented using ECRL logic with cross-coupled PMOS transistors as shown in the Fig. 7. The two inputs are a and b and z is the output of the gate.

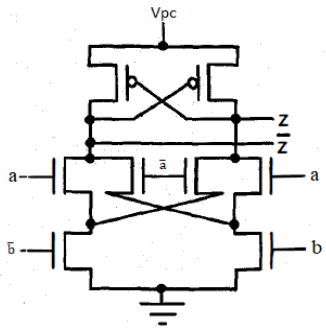

Fig. 7. ECRL XOR/XNOR gate

Fig. 8 gives the implementation of the D-flip-flop using ECRL logic. The edge triggered flip flop changes states Either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse on the control input.

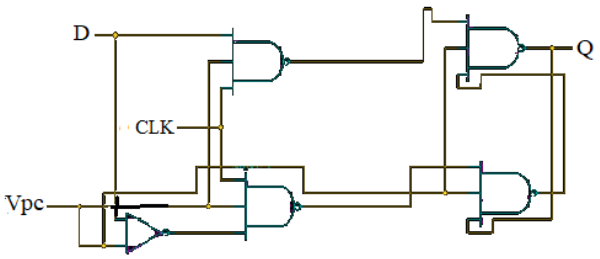

Fig. 8. ECRL D flip-flop

The schematic diagram of ECRL full adder is shown in Fig. 9. This circuit consists of both NAND and XOR gates shown in figures 6 and 7 respectively. As shown, the full adder accepts the inputs a, b, and c and produces sum and carry as outputs.

Fig. 10 shows the implementation of a 4-bit pipelined carry save adder using ECRL logic. This circuit makes use of full adders and D-flip-flops as building blocks.

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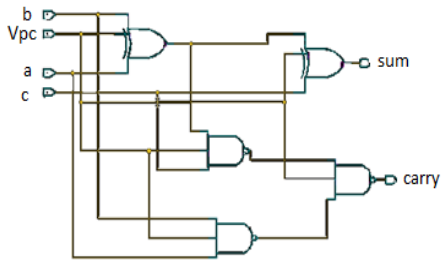

Fig. 9. ECRL full adder

The ECRL logic reduces the power dissipation and pipelined architecture improves the speed of the adder.

V. Results

The designed circuits are simulated using Mentor Graphics tool at 130nm technology node. The effect of pipelining on the speed of the adder is verified by performing delay analysis on the static CMOS carry save adder circuits implemented without and with pipelining. Table 1 gives the delay values of the conventional and pipelined CMOS adder circuits. An improvement of 99.4% in speed is observed with pipelining. Table 1 also lists the power dissipation values for both pipelined static CMOS and ECRL adders. The results indicate a reduction of 46.3% in power dissipation for the ECRL adder as compared to CMOS circuit.

TABLE 1 Comparison of delay and power dissipation of Static CMOS and ECRL adder circuits

Parameter	**4-bit static CMOS carry save adder**	**4-bit pipelined carry save adder using CMOS logic**	**4-bit pipelined carry save adder using ECRL**
Delay (ns)	50.058	0.2705	---
Power dissipation (μW)	339.74	511.44	274.38

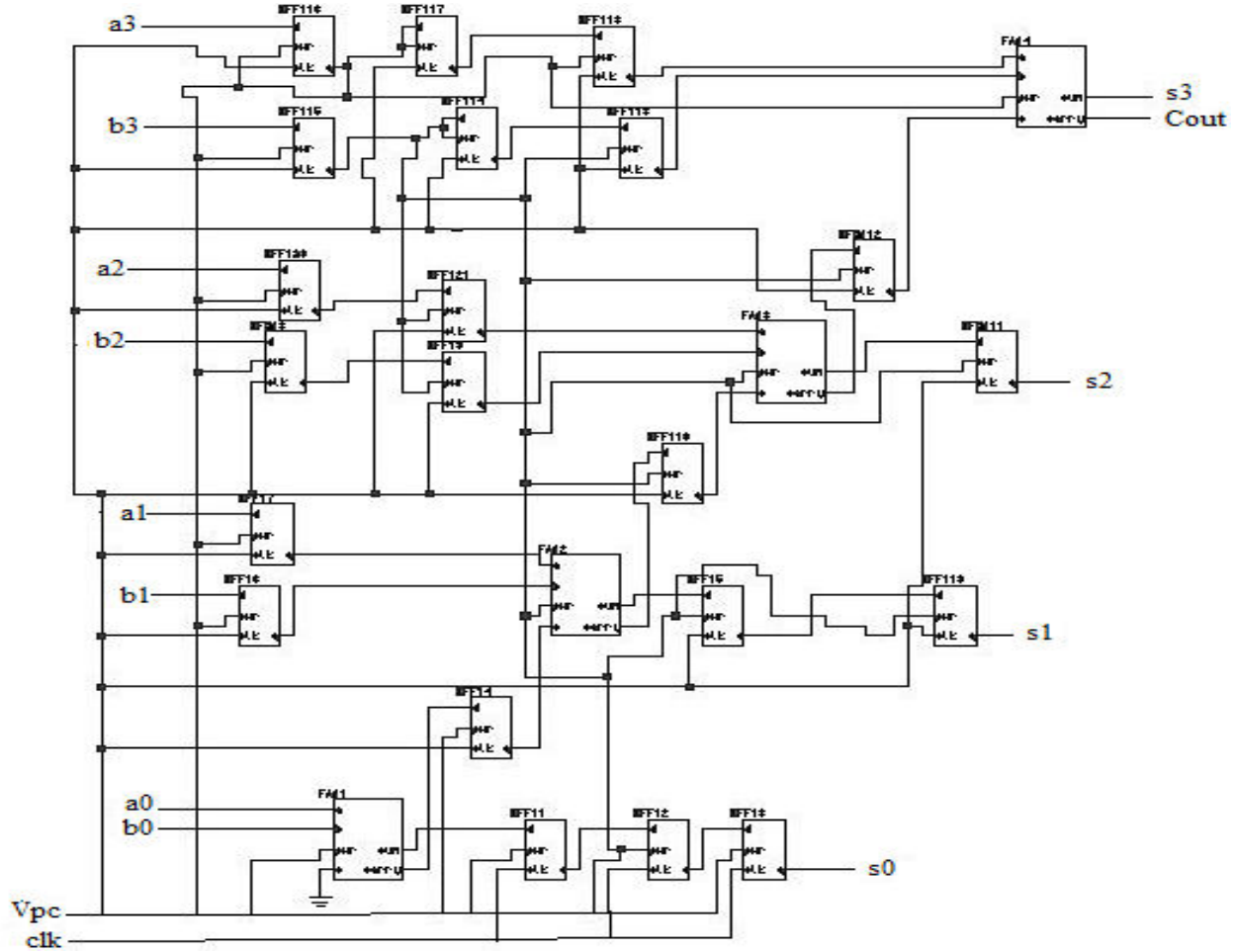

Fig. 10. 4-bit pipelined carry save adder using ECRL logic

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VI. Conclusion

In this work, a 4-bit carry save adder is designed and implemented using conventional CMOS logic, without and with pipelining. The simulations using Mentor Graphics tool at 130 nm technology node indicate an improvement of 99.4% in speed with pipelining. In order to lower the power dissipation, adiabatic ECRL logic is used to design and implement the 4-bit carry save adder using pipelining. The power dissipation of this configuration is found to be reduced by 46.3% as compared to conventional CMOS pipelined adder. Thus it can be concluded that pipelining approach and adiabatic ECRL logic can be conveniently used to design high speed and low power adder circuits suitable for portable and battery operated devices.

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Author's Profile

T. Srinivasa Rao has obtained his B.Tech. in Electronics and Communication Engineering from Jawaharlal Nehru Technological University Kakinada. His areas of interest are digital electronics and low-power VLSI.

S. Sai Teja Sri has obtained her B.Tech. in Electronics and Communication Engineering from Jawaharlal Nehru Technological University Kakinada. Her areas of interest are digital electronics and low-power VLSI.

***A. V. N Tilak** had obtained his Masters degree from Indian Institute of Technology, Kanpur and Ph.D. from Indian Institute of Technology, Madras during 1984 and 1997 respectively. He is a Member of IEEE, Fellow of Institution of Electronics and Communication Engineers (IETE), Fellow of Institution of Engineers (India). He is also life member of Indian Society for Technical Education (ISTE). He is presently working as a Professor of Electronics and Communication Engineering and Dean-PG Studies, R&D and Consultancy at Gudlavalleru Engineering College, Gudlavalleru, India.*