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Energy Efficient 7T SRAM Design For Improved Speed of Application

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Abstract *– The need for low power integrated circuits is well known because of their extensive use in the electronic portable equipments. On chip SRAMs (Static Random Access Memory) determine the power dissipation of SoCs (System on Chips) in addition to its speed of operation. Hence it is very important to have energy efficient SRAMs. This Thesis proposes energy efficient SRAM cells (7T) based on adiabatic principles and design modifications.*

Bulk of the energy in SRAMs is wasted during charging of the bit lines and discharging it to the ground during read and writes operations. It is proposed to use adiabatic approach to collect this energy and recycle it. Based on this thought process a separate and simple adiabatic driver circuit has been designed and used for bit line charging. It is shown that in 6T SRAM, a total energy of the order of 50% over a given period and around 80% during write cycle can be saved by the help of this driver.

With this adiabatic driver circuit working in conjunction with conventional 7T SRAM cell other performance characteristics like read stability, write ability, read and write delay etc have been found by simulation in addition to energy saving under varied conditions of memory operations. The effect of device parameters of the driver on total energy of the SRAM cell has been investigated. Further studies covered proposed SRAM cell arrays. With a view to increase energy saving further, the possibility of having adiabatic SRAM with single bit line for reading and writing is examined. This architecture improves the total energy saving further (90%). Feat SRAM is designed to get better speed of operation along with energy saving.

Keywords*: Brain Wave Analysis ; Sounds & Vibration ;HUMAN ENGINEERING ; Working Efficiency of Employees ; Productivity*

I. INTRODUCTION

The growing demand of portable battery operated systems has made energy efficient processors a necessity. For applications like wearable computing energy efficiency takes top most priority. These embedded systems need repeated charging of their batteries. The problem is more severe in the wireless sensor networks which are deployed for monitoring the environmental parameters. These systems may not have access for recharging of batteries. We know that on chip memories determine the power dissipation of SoC chips. Hence it is very important to have low power and energy efficient and stable SRAM which is mainly used for on chip memories.

There are various approaches that are adopted to reduce power dissipation, like design of circuits with power supply voltage scaling, power gating and drowsy method. Lower power supply voltage reduces the dynamic power in quadratic fashion and leakage power in exponential way. But power supply voltage scaling results in reduced noise margin. Many SRAM arrays are based on minimizing the active capacitance and reducing the swing voltage. In sub-100nm region leakage currents are mainly due to gate leakage and sub threshold leakage current. High dielectric constant gate technology decreases the gate leakage current. Forward body biasing methods and dual Vt techniques are used to reduce sub threshold leakage current. In sub threshold SRAMs power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

The energy loss during writing is more than the energy loss during reading in conventional SRAM since there is full swing of voltage in bit lines whereas the bit line voltage swing is very less during reading. It is known that the energy stored in the bit lines of the conventional SRAM is lost to ground in each write operation during ‘1’ to ‘0’ transition and this is the main source of energy loss. The power dissipated in bit lines represents about 60% of the total dynamic power consumption during a write

operation. The power consumption by bit lines during writing is proportional to the bit line capacitance, square of the bit line voltage and the frequency of writing.

Energy loss is reduced by limiting voltage differences across conducting devices. This is accomplished through the use of time-varying voltage waveforms. This is also called Adiabatic charging technique. The SRAM working purely on adiabatic charging principles need multiple phase power clocks. Although there is huge saving in energy during writing as well as reading, the design of the SRAM circuit is complex and not same as the design of conventional SRAM. The latency of operation is more.

There is a powerful approach in which the energy stored in the bit line capacitance that is normally lost to ground is collected and pumped back into the source. This is known as energy recovery approach. Based on the phase of the charging source, pre charging techniques, sense amplifier, the complexity and area of the pumping circuit there are variants.

To overcome the design complexity and latency of complete adiabatic SRAMs, SRAMs that make use of adiabatic charging technique partially have been designed. Based on whether adiabatic charging is applied to only power supply line or ground line or bit lines and word lines or only bit lines, there are many types of adiabatic SRAMs . High resistivity switches are also used to vary the power supply voltage slowly.

Energy stored in the bit lines is recycled by the help of switches to adjacent bit lines in order to save energy in bit line charge-recycle method. This method reduces the swing voltages to a low swing voltage. Based on whether energy recycling is done only during writing cycle or during both writing and reading cycles, there are variants.

It is necessary that in addition to saving energy in SRAMs care should be taken to see the performance parameters are not much affected. In this Thesis an attempt has been made to recover energy stored in the bit lines and reused it by adiabatic principles. This has been made possible by using a very simple, small and efficient adiabatic driver for charging and discharging the bit lines. The adiabatic driver is driven by a D.C shifted single phase sinusoidal power clock which enables the charging and discharging of the bit lines based on the signal which is 'DATA' AND 'WE' input. Hence the loss of energy to the ground during '1'to'0' transition in SRAM is reduced to a great extent. No separate pre charging circuit is used before or after reading. No synchronization circuit is needed as only bit lines are concerned. Low power sense amplifier is utilized to sense the data. The design of the conventional SRAM can be retained except the write driver and the pre charge circuit. With this adiabatic driver circuit working in conjunction with conventional 6T SRAM cell other performance characteristics like read stability, write ability, read and write delay etc have been found by simulation in addition to energy saving under varied conditions of memory operations. The effect of device parameters of the driver on total energy of the SRAM cell has been investigated. Further studies covered proposed SRAM cell arrays.

In addition to recovering the energy from both bit lines the possibility of operating the SRAM cell with single bit line driven by an adiabatic driver is examined to save energy. This effort has resulted in realizing adiabatic 5T SRAM cell which consumes significantly lower energy than adiabatic 6T SRAM cell with reduction in bit line leakage power and with better Static Noise Margin (SNM). Single ended reading is employed and this does not need pre charging, which saves energy. Further the design of adiabatic 5T SRAM is modified to get Feat SRAM which has better speed of operation in addition to other performance parameters remaining almost the same. All these investigations have been carried out using HSPICE simulator with 65nm PTM models. The Thesis deals with the description of the effort put in to arrive at energy efficient adiabatic 6T and 5T SRAM cells whose other performance characteristics are almost comparable to those of 6T conventional SRAM cell.

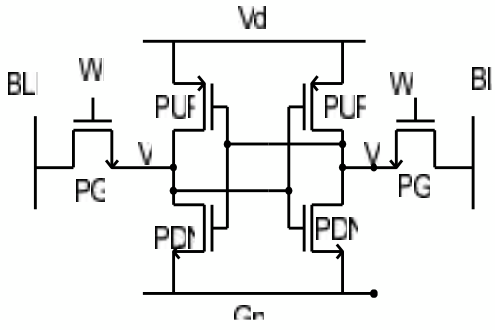

Figure 1 Circuit diagram of SRAM

II. LITERATURE SURVEY

These investigations cover SRAMs operated at low voltages reducing power dissipation, SRAMs using techniques like power gating in which the circuits are switched off when they are not needed , SRAMs (drowsy) where the power supply voltage is reduced to a lower value during standby mode and SRAMs based on adiabatic techniques. Lowering the power supply voltage reduces the dynamic power quadratically and leakage power exponentially. But power supply voltage scaling also limits signal swing and thus reduces noise margin. Further, aggressive technology scaling in the sub-100nm region increases the sensitivity of the circuit parameters to process variation (PV). Leakage currents are mainly due to gate leakage current and sub threshold leakage current. High K gate technology decreases the gate leakage current. Forward body biasing methods and dual Vt techniques are used to reduce sub threshold leakage current. In sub-threshold SRAMs, power supply voltage (VDD) is lower than the transistor threshold voltage (Vt) and the sub threshold leakage current is the operating current.

Tae-Hyoung Kim *et. al* [14] introduced various circuit techniques for designing robust high density sub threshold SRAMs: (i) decoupled cell for read margin improvement, (ii) utilizing reverse short channel effect (RSCE) for write margin improvement, (iii) eliminating data dependent bit line leakage to enable long bit lines, (iv) virtual ground replica scheme for improved bit line sensing margin, (v) write back scheme for data preservation during write, and (vi) optimal gate sizing based on sub threshold logical effort. To achieve all these operations the authors pro- posed 10T SRAM cell operating in sub threshold region that has an SNM of 76mV at a supply voltage of 0.2V while that of a conventional 6T SRAM cell is 14mV. It improves the cell write ability without introducing a separate high VDD. Reverse short channel effect yields further advantages such as better sub threshold slope owing to the longer channel length and reduced impact of random doping fluctuation due to the increased gate area for equal drive current. A SRAM of 480kb cells was fabricated in 0.13µm CMOS technology. As per the measured results leakage current consumption is reported to be 10.2µA at supply voltage equal to 0.20V at 27°C. The normalized virtual ground voltage was found to rise significantly as the supply is reduced and the number of cells per bit line increased (i.e., 50% of VDD at 0.20V, 1024 cells). A 6% change in virtual ground voltage was measured when the temperature is varied from 27°C to 80°C.

Jaydeep P. Kulkarni *et.al* [15] proposed Schmitt Trigger SRAM cell that incorporates a built-in feedback mechanism, achieving 56 % improvement in SNM, improvement in process variation tolerance lower read failure probability, low-voltage/low power operation, and improved data retention capability at ultra low voltage compared to conventional 6T SRAM cell. They report that at iso-area and iso-read-failure probability the proposed memory bit cell operates at a lower (175 mV) VDD with 18% reduction in leakage and 50% reduction in read/write power compared to the conventional 6T cell. As per their simulation results, the proposed memory bit cell retains data at a supply voltage of 150 mV. Functional SRAM with the proposed memory bit cell was demonstrated at 160 mV in 0.13µm CMOS technology.

SRAM is preferred in “on chip memories” due to its speed of operation. On chip memories contribute to a large part of power consumption of System on Chips (SoCs). The energy loss in memories is due to bit lines, word lines, address decoders and peripheral circuits. The energy losses in bit lines is during pre-charge, read and write cycles and in word lines the energy loss takes place whenever a line is accessed. The energy loss due to charging and discharging of bit line capacitance during write operation is significant. During write operation, for the ‘1’ to ‘0’ transition at the storage node, the corresponding bit line discharges to the ground. The energy loss due to complete discharge is equal to $1/2CV^2$ (where ‘C’ is the capacitance of the bit line and ‘V’ is the bit line voltage). During read operation the charges from the bit line connected to the node storing ‘0’ discharges the charges through the pull down N-MOSFET. The energy loss during read operation can be made lesser by reducing the time of discharge or by controlling the drop in the bit line voltage. The sense amplifiers help in giving out proper voltage levels after detecting a small voltage difference of the order of few mV.

III. PROPOSED METHOD

In this work it is opted to reduce the energy losses by pumping the energy from the bit lines of SRAM into the power clock by using a simple energy recovery driver. A typical SRAM cell is shown in Fig. 2. The energy recovery system has a power clock separate from the main supply and has an energy recovery driver as shown in Fig. 3. The energy recovery driver circuit consists of an N and a P MOSFET connected to the capacitance load

through diodes. When the input signal say 'DIN' is high, the N-MOSFET turns on. The capacitance charges to the peak value of the power clock voltage 'VPC' minus the voltage drop across the conducting path through the diode 'D1'. When the input signal is low, the P-MOSFET turns on. The excess charge stored in the capacitance is pumped back to the signal generator through diode 'D2' when the capacitor voltage is higher than the power clock voltage and the voltage drop across the conducting path. The voltage drop across the diode and the MOSFET is very small voltage as the polarities of the diode drop is in such a way that it cancels with the threshold voltage of the MOSFET. Hence there is less loss of energy. In order to make use of these drivers to save energy in bit lines, two drivers are needed one for each of the bit lines. The energy saved is proportional to $1/2CV^2$ (where 'C' is the capacitance of the bit line and 'V' is the bit line voltage). The bit line capacitance depends on the number of rows and the technology. Energy dissipated in driving the load capacitance can be reduced by employing slowly varying signal such as triangular, shifted sinusoidal etc as power clock. We have considered sinusoidal signal source with a dc shift of value equal to half of power supply voltage mainly because of ease of generation. This amounts to charging the capacitor in incremental steps of infinitesimally small step size ΔV over k steps where k tends to become very large number. The energy saving is proportional to k.C. $\Delta V^2/2$. A single sinusoidal signal source is sufficient for the entire SRAM array. Many oscillators are reported in the literature for use in adiabatic circuits with considerable conversion efficiencies. One such oscillator reported claims efficiencies in excess of 90%. The operation of this oscillator with 65nm technology is verified. However for energy saving analysis purpose a power clock of 100% efficiency is considered in this Thesis. In adiabatic SRAM these two circuits shown in Fig. 2 and Fig. 3 are combined. The following section describes an adiabatic SRAM cell.

In the proposed SRAM scheme the MOSFETs and the diodes in the driver, enable charging and discharging of the bit line. The power clock uses a clamped sinusoid with a frequency of the order of 10MHz (100MHz for larger arrays) to charge the bit lines. Power clock is utilized to pre-charge the bit lines before reading operations are carried out. The efficiency of the power clock is assumed to be 100%. In this circuit one can ensure that both the bit lines are charged to the same voltages before reading. The various steps involved in writing, reading and hold operations in the new circuit are given below.

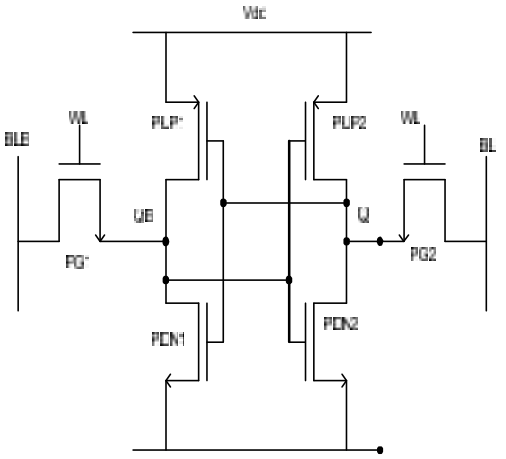

Figure 2. 7T SRAM cell

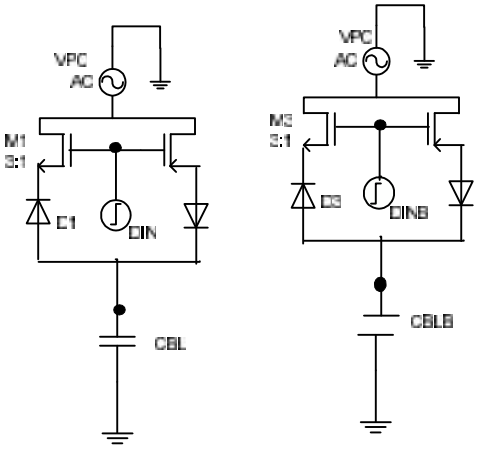

Figure 3. Proposed drivers for bit lines

In both the conventional SRAM and the proposed adiabatic SRAM, the data which has to be written is first obtained with its complement using two inverting buffers as shown in Fig. 5.3b. The data and its complement is applied to AND circuits separately which produce complement outputs only when write enable signal 'WE' is active as shown in Fig.5.3c. This ensures that the data is applied to the bit lines only when the write operation is enabled. The signals obtained from the AND circuits are represented by 'DIN' and 'DINB' respectively in Fig.5.3a. The first step in the write operation is to apply the data 'DIN' and 'DINB' to the bit lines through the energy recovery driver unlike in the case of conventional one where it is applied through driver transistors.

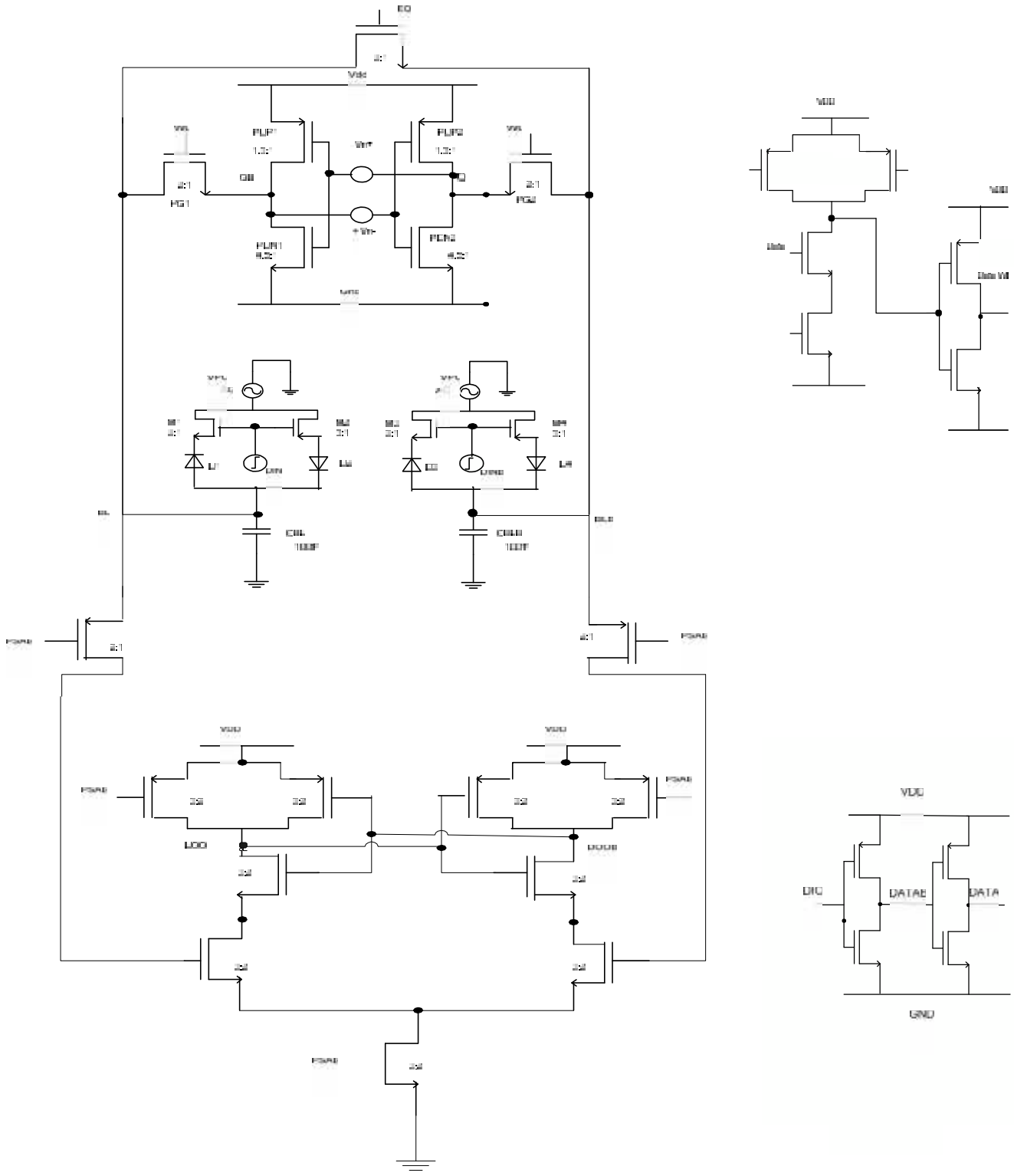

Figure 4 Adiabatic SRAM system

When the input signal 'DIN' is low, the bit line capacitance 'CBL' charges to the peak voltage of the power clock voltage through diode D2.However the maximum voltage of the bit lines is limited by the drop across the P-MOSFET switch that connects the sense amplifier to the bit lines When the input signal 'DIN' is high, the bit line capacitance 'CBL' discharges to the power clock through diode D1. Complimentary action takes place in the other bit line 'CBLB'. The access transistors are then enabled by activating the word line WL line. The data on the bit lines are passed to the SRAM by the access transistors. Most of the energy from the bit line connected to the storage node which undergoes'1' to '0' change gets back into the power clock through the energy recovery driver. Where as in the conventional SRAM it goes to the ground and gets wasted. Thus in this new SRAM the energy that is usually lost during writing operation is partially recovered.

Separate pre-charging circuit is not used for the proposed SRAM. Pre-charging is done prior to read operation as both DIN and DINB are equal to '0' as write enable is now equal to '0'. Both the bit lines CBL and CBLB are maintained at the same potential before the word lines are activated. In case of read operation normally one of the bit lines is allowed to discharge to the ground by a small percentage (less than 10% of the bit line voltage) and this energy, is relatively less. However it is wasted as in the case of conventional circuit.

The sense amplifier used is current –mode latch sense amplifier [69]. The current flow of two sense amplifier input N-MOSFETs whose gates are connected to bit lines BL and BLB controls the serially connected latch circuit. The leakage energy of one sense amplifier alone is found to be 1.1756e-16J.

During the 'Hold' operation the access transistors are disabled and the condition of the adiabatic SRAM would be similar to that of conventional SRAM. The bit lines are charged to maintain the peak voltages of the power clock reduced by the drop across the switch connecting the sense amplifier to the bit line as the write enable signal 'WE' is low.

IV. RESULT

The performance of the energy saving 7T SRAM cell is compared with 7T SRAM cell without adiabatic driver. The parameters considered are total energy, write delay, read delay, static noise margin, write margin and leakage power. The performance parameters are tabulated in Table 1.

The total energy consumed by the system includes the energy drawn by the SRAM, reading and writing circuitry. Since CMOS circuits are used in all the systems, static power dissipation is almost the same in all the systems. But the difference arises because of active power which is due to writing and reading. Energy consumed during reading is almost the same in both the non adiabatic and the adiabatic SRAMs because the charges flow from the bit line connected to the node storing '0' through the pull down NMOS transistor into the ground. The quantity of energy lost during reading however is controllable by restricting the time of discharge. The energy lost during writing is pumped back and is saved in the proposed adiabatic SRAMs. It is found that around 53% of total energy is saved by adiabatic 7TSRAM when compared to the non adiabatic type.

Table 1 Performance comparison of 5T adiabatic SRAM with 5T non adiabatic SRAM.

SRAM	Non adiabatic 5T	Adiabatic 7T
Total energy(n J)	0.072284	0.019995
SNM (V)	0.357	0.357
Write margin (V) 0 to 1	0.669	0.669
1 to 0	0.72	0.72
Read delay(ns)	1.48	1.5
Write delay(ns)	1.22	12.07
Leakage power(pw)	0.24	0.06

The threshold voltage as per the PTM model considered is -0.471V for PMOSFET and 0.516V for N-MOSFET. The value of standard deviation for threshold voltage of the MOSFET is taken to be 30mV (approximately 8% of the threshold voltages) and the random variation of Gaussian

type is assumed. The power supply voltage is taken as 1.1V and a 10% of this which is 110mV is taken as the sigma for the random variation of Gaussian type of the power supply voltage. Using these parameters, Montecarlo simulations(1000) in Tanner have been carried out to find the spread of total energy consumed, SPNM, WTP, read delay and write delay both for conventional and adiabatic SRAM cell at room temperature. The distribution of total energy of non adiabatic 7T SRAMs cell and that of adiabatic SRAM cell.

Table 2
Mean and standard deviation of non adiabatic 7T SRAM

Non adiabatic 7TSRAM cell		
Performance	Mean(μ)	Standard Deviation(σ)
Total energy(n J)	0.042	0.0113
SNM (V)	0.277	0.029
Write margin (V) 0 to 1	0.125	0.109
1 to 0	0.127	0.109
Read delay(ns)	0.9	0.349
Write delay(ns)	3.96	0.437

The 5T adiabatic SRAM cell with single ended read amplifier is compared with symmetrical 7T SRAM cell with double ended read amplifier with respect to its performance parameters. In order to boost SNM, the asymmetry of the 5T SRAM is chosen. When the total energy of the adiabatic 5T SRAM cell and the conventional SRAM cell is compared, it is found to be 0.017X that of conventional 6T SRAM cell. It is seen that 98.2 % energy is saved with respect to non adiabatic 7T symmetrical SRAM. The performance parameters are tabulated in Table 3. The static noise margin is improved in 5T SRAMs. Due to the asymmetry in 5T SRAM, the 0 to 1 write margin is different from 1 to 0 write margins. The write margin is more in both types of 5T SRAMs due to the difference in pull up ratios. With same bit line capacitance, the read delay is less in both the types of 5T SRAMs due to reduced input capacitance of the single ended read amplifier. Write delay is greater in adiabatic SRAMs (both 7T and 5T) when compared to their respective non adiabatic versions due to increased write circuit resistance.

Table 3 Comparison of total energy of 5T adiabatic SRAM with that of symmetrical conventional 7T SRAM cell

SRAM	Non adiabatic 7T	Adiabatic 7T	Non adiabatic 5T	Adiabatic 5T
Total energy(J)	$2.995X10^{-9}$	$1.189 X10^{-9}$	$11.19x10^{-11}$	$5.2x10^{-11}$
SNM (V)	0.188	0.188	0.357	0.357
Write margin (V) 0 to 1	0.655	0.655	0.669	0.669
	0.655	0.655	0.72	0.72
Read delay(ns)	8.76	3.81	1.48	1.5
Write delay(ns)	10.35	64.98	1.22	12.07

V. CONCLUSION

Several groups are working in developing memories with low power dissipation and high efficiency. SRAMs are known to dissipate high power. They are indispensable in several applications that include System on Chips (SoCs). Therefore attention is paid towards developing low energy and high efficiency SRAM cells and architectures. This Thesis attempts at developing low energy high efficiency SRAM cells and arrays

through the application of energy recovery and adiabatic principles keeping the performance parameters in the same order as that of conventional SRAM. Experimental study of low power SRAMs has been done as preliminary work.

It is known that bulk of the energy is wasted in SRAMs through the charging and discharging of bit lines. It has been shown that by providing an adiabatic charging circuit for the bit line charging, energy which normally would have got wasted would be recovered and hence results in relatively low energy SRAM cells. The design of the proposed adiabatic SRAM is simple with no need of synchronization as only bit lines are concerned. The voltage drop across the adiabatic driver is negligible. This adiabatic 7T SRAM do not use separate pre charge circuit and do not need any major changes in the conventional SRAM design.

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