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High-Speed and Energy-Efficient Carry-Skip-Adder Design

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Abstract *– The importance of energy-efficient processor design is recognized in designing of Ultra low power processor design. CSKA structure presented here is able to achieve a very high speed in comparison to normal carry skip adder. The most prominent application of proposed structure is in the field of ALU design for microprocessors. Main focus of this work is on the synthesis and simulation of high speed adders. These high speed adders are designed using different architecture as the basic building blocks for complete structure on Vivado using VHDL language and the results are further compared with several other adder structures. These high speed adder structures not only minimize the total energy consumption of the system but also reduce the time taken by each arithmetic operation i.e. increase the system operating speed. A CSKA structure is proposed in [1], the presented structure is both Power and area efficient. Total path delay of the CSKA is smaller as compare to that of RCA and CLA. Area requirement of CI_CSKA is high as compare to the RCA and CLA, while power delay product of this CI_CSKA structure presented in this paper is less among the three.*

Keywords*: High Speed Adder, Concatenation Incrementation (CI), Carry skip adder (CSKA), CLA, RCA, Hybrid Structure, Concatenation and Incrementation Carry Skip Adder (CI_CSKA), Brent Kung (BK), Kogge Stone, Parallel Prefix Adder (PPA)*

I. Introduction

The Carry Skip adder structure is present in literature since early 1960s. Carry Skip Adder is very efficient for designing the adder structure with very higher number of input bits. CSKA is made-up of small sub-blocks i.e. several small RCA adder blocks and skip logic. Since, in RCA blocks carry bit is propagated from input to the output by rippling from each stage, we have replaced the RCA blocks by CLA blocks. In CLA structure carry bit is computed separately, so output carry is available for next block by the time sum output of present block is out. One more technique to improve the speed of the adder is presented in [1]. This scheme is known as Carry skip technique and the resultant structure is known as CSKA. In the concatenation and incrementation scheme presented in [2] the delay of carry skip logic block is improved.

The main components of the CI_CSKA structure are summarized as follows:

- Adder blocks
- Skip Logic
- Concatenation and Incrementation block

Exact amount of delay and power can be obtained only after the completion of design process and simulation. Therefore, there is always an uncertainty about whether low power or high speed design can be obtained using other topology. Transistor sizing, routing parasitic, load effects and power should be the main consideration for starting any design.

II. Previous Work

In the paper "A Family of Adders" [3] author present the study of different adder topologies and shows how they influence the wiring density and fan-out of the circuit, which is further responsible for estimating area/power tradeoffs. Chan et al. [4] in "Delay optimization of Carry Skip adders and Block Carry Lookahead adders using Multidimensional Dynamic programming" shows the impact of structural grouping of full adders as small blocks on the propagation delay. They have also worked on the number of levels that can be used for grouping the smaller blocks. This Multidimensional dynamic programming will result in minimum latency. In this report for the calculation of total critical path delay they have proposed a delay model

which is using fan-in, fan-out as two major constraints with the intrinsic gate delays.

To optimize the parallel prefix adder, Wei et al. [5] used the concept of dynamic programing techniques. Wei in his paper worked on 66-bit adder using floating point processor. The adder designed by them is optimized with respect to the area-time.

Basic components of the conventional CSKA structure are FAs chain and skip-logic blocks. Skip logic consist logic gates and multiplexer. CSKA can be made in one or more level by placing the 2:1 multiplexer in different levels [6]. They have also have proposed a method to find the optimal number of full adders in each stage. Lee in his paper discussed on varying the block size of a block carry-lookahead adder [7]. Optimization of the carry propagation delay for large size adders, by further varying the state size is very useful technique.

In the basic structure of carry skip adder, FAs chain and logic gates are used to determine the skip action. In case when carry bit has to propagate through all the FAs then ripple carry adder suffers from the worst case delay. Which leads to the worst case propagation delay for Carry skip adder too. The carry output of each RCA block is similar to that of input. It means that the delay will be proportional to the number of FAs in that chain. In the carry skip adder, skip logic blocks are used to detect these kinds of situations and made the carry bit available for the next stage instead of waiting for the computation of carry from previous FAs chain as in case of RCA. FAs in CSKA formed smaller group of FAs chain results in number of stages. Each stage contains an RCA block and a skip logic block. Carry output of FAs chain and carry input of each stage are two inputs of the skip logic. Whether the carry will be propagate or not, depends on the select signal. Select signal is product of the propagation signals of that stage.

The carry skip adder can be designed using FSS or VSS structures. Variable state size structure will be able to achieve the highest speed [6], [8].

Several researchers have worked in the field of digital design to optimize the speed and power consumption of the adders and other arithmetic units i.e. subtractor, multiplexers etc. Some of the work which is carried out on adders has been reported in [9]-[11] also.

III. Tables and Figures

Table I shows the comparative study we have done in this work. We have designed five structures RCA, CLA, Conventional CSKA_RCA, CI_CSKA_RCA and FSS Hybrid_KS CI_CSKA_CLA for the study. Times taken to compute the output sum using all of these structures are presented in Table I. We have also listed the power consumption of each of these structures.

Form the table we can easily draw a conclusion that the proposed structures are far better in terms of performance compare to the conventional structures. Speed of the hybrid structure is very high compare to all other structures.

Fig.1 shows the comparison of the delay time for different structures. Fig.2 shows the total On-chip power consumption. Basic structure of the Conventional Carry skip adder is shown in the Fig.3.

TABLE I

Adder Structure	Delay (ns)	Power (W)
RCA	26.344	23.531
CLA	25.581	23.584
Conventional CSKA_RCA	22.368	23.657
CI_CSKA_RCA	23.452	25.382
FSS Hybrid_KS CI_CSKA_CLA	18.605	24.815

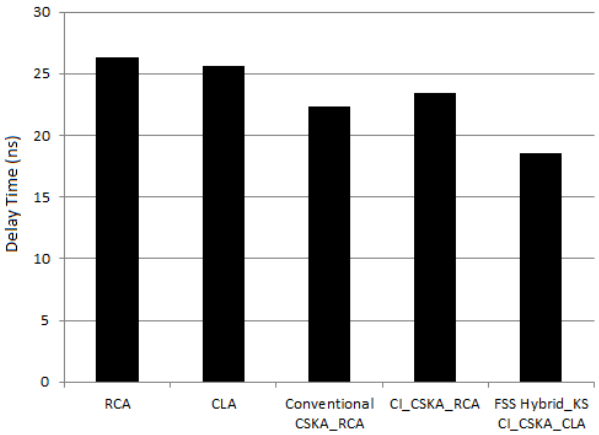

Fig. 1. Delay time Comparison

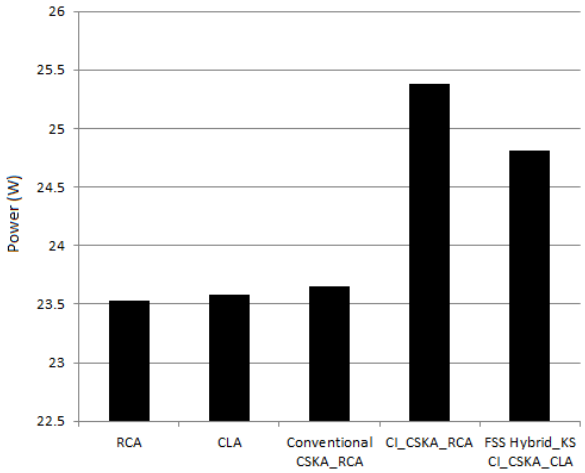

Fig. 2. Total On-chip power Consumption

Proposed hybrid structure of CSKA is shown in Fig.4. In the Hybrid CI_CSKA_ using CLA blocks shown in Fig. 4, the carry input is zero for each CLA block, except from the first block where, carry input is Ci.

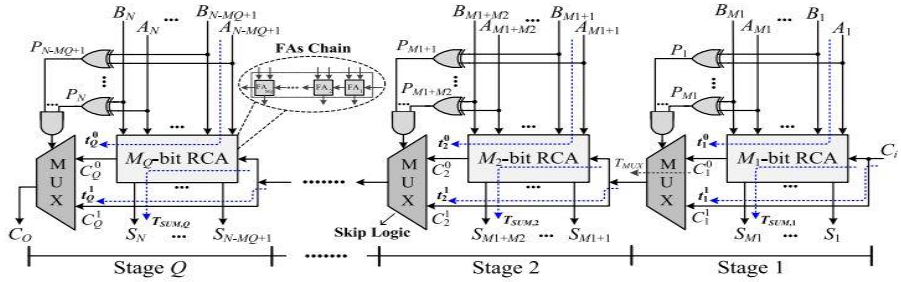

Fig. 3. Conventional CSKA Structure

This arrangement of blocks will result in the concatenation. In the concatenation scheme each CLA block do not have to wait for the input carry from previous stage.

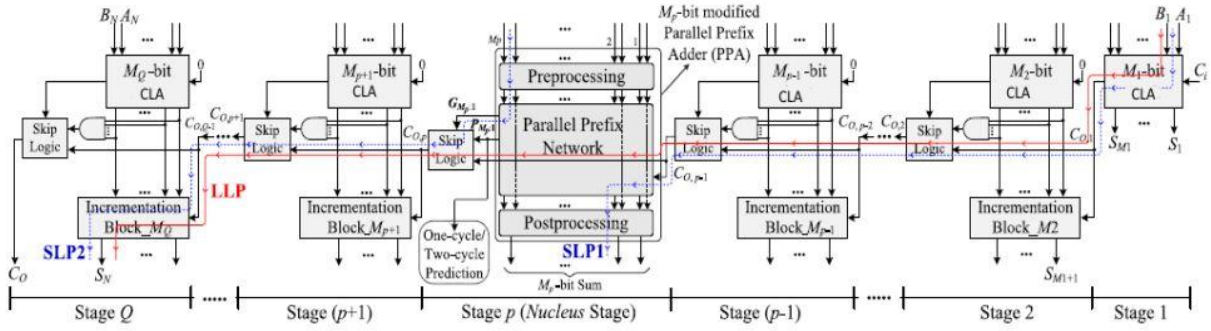

Fig. 4. Hybrid CI_CSKA_CLA Structure

IV. Simulation Results

The simulations for all these structures are done using VIVADO Design Suite 16.2 and the targeted family for the simulation on FPGA is Artix-7. This work involves the designing of a RCA, CLA, Conventional CSKA_RCA, CI_CSKA_RCA and FSS Hybrid_KS CI_CSKA_CLA structure using small size RCA and CLA blocks along with a PPA block. The energy efficient algorithm which is proposed here is implemented using VHDL language. All these design structure in this paper are compared on the basis of two performance metrics path delay and total On chip power dissipation. Results that we have obtained shows that both of the performance metric, the path delay and total on chip power of the proposed hybrid structure are better than the RCA, CLA, basic carry skip adder, and CI carry skip adder proposed in [2]. The simulation output of designed structure is shown in Fig.3. Waveforms shown in Fig.3 are simulation result of the adder structure. There will be some ambiguity at the starting of the output waveforms due to the delay produced by the adder in the synthesized simulation output. When we use CLA blocks for addition, the delay that will be present is mainly because of the routing used for each gate.

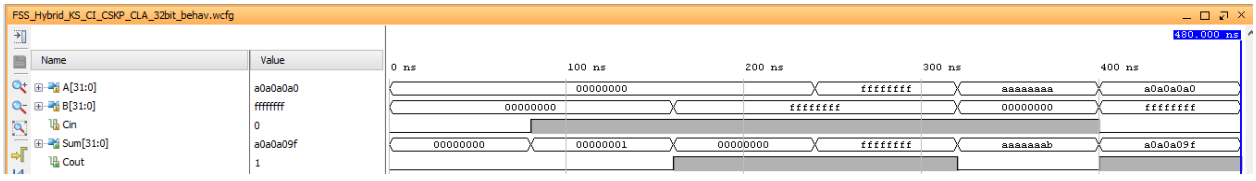

Fig. 5. Simulated Waveforms

V. Abbreviation

Concatenation Incrementation (CI), Carry skip adder (CSKA), Carry Lookahead Adder (CLA), Ripple Carry Adder (RCA), Concatenation and Incrementation Carry Skip Adder (CI_CSKA), Parallel Prefix Network (PNN),

Parallel Prefix Adder (PPA), Brent Kung (BK), Kogge Stone (KS), fixed state size (FSS), variable state size (VSS).

CKSA_RCA: Carry skip adder using RCA blocks
CSKA_CLA: Carry skip adder using CLA blocks
Hybrid_BK : Using Brent kung PPN at central stage
Hybrid_KS : Using Kogge Stone kung PPN at central stage.

VI. Conclusion

High speed and energy efficient architecture of Hybrid CI_CSKA is proposed in this paper. The simulation results showed that the proposed hybrid architecture has better performance in terms of speed and total energy consumption compared to the existing one. The proposed structure has fixed state size of CLA blocks and is an energy efficient structure for addition. Hybrid CI_CSKA is able to achieve very small value of delay but since Carry lookahead adder has complex structure, it needs extra gates, which will cost us in term of area requirement. With some modifications in design structure i.e. variable state size, use of other PPN etc. performance of this adder can be further improved. Area, delay, energy consumption, routing complexity can be the metrics which can be used to analyze in future work for the performance analysis of the CI_CSKA. In present work we have done analysis of 32 bit adder. In future work we can increase the number of bits and analyze the performance.

References

[1] M. Lehman and N. Burla, Skip techniques for high-speed carry propagation in binary arithmetic units, *IRE Trans. On Electronic Computers, Vol. EC-10,* no. 4, pp. 691–698, 1961.

[2] Milad Bahadori, Mehdi Kamal, Ali Afzali-Kusha et. al., High-Speed and Energy Efficient Carry Skip Adder Operating Under a Wide Range of Supply Voltage Levels, *IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 24,* no. 2, pp. 421–433, 2015.

[3] Simon Knowles, A family of adders, *in Proc. 14th Symp. Computer Arithmetic*, Adelaide, Australia, Apr. 1999, pp. 30–34.

[4] P. K. Chan, M. D. F. Schlag, C. D. Thomborson, and V. G. Oklobdzija, Delay optimization of carry-skip adders and block carry-lookahead adders using multidimensional dynamic programming, *IEEE Trans. Comput., vol. 41*, no 8, pp. 920–930, Aug. 1992.

[5] B. W. Wei and C. D. Thompson, Area-time optimal adder design, *IEEE Trans. Comput*., *vol*. *39*, no. 5, pp. 666-675, 1990.

[6] M. Alioto and G. Palumbo, A simple strategy for optimized design of one-level carry-skip adders, *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl., Vol. 50,* no. 1, pp. 141–148, Jan. 2003.

[7] B. Lee, VLSI implementation of fast arithmetic algorithms: Optimizing delays in carry lookahead adders, CS*2921: Class project rep., U.C. Berkeley,* 1989.

[8] S. Turrini, Optimal group distribution in carry-skip adders, in *Proc. 9th IEEE Symp. Comput. Arithmetic,* Sep. 1989, pp. 96–103.

[9] V. G. Oklobdzija, B. R. Zeydel, H. Q. Dao, S. Mathew, and R. Krishnamurthy, Comparison of high-performance VLSI adders in the energy-delay space, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 13,* no. 6, pp. 754–758, Jun. 2005.

[10] R. Zlatanovici, S. Kao, and B. Nikolic, Energy–delay optimization of 64-bit carry-lookahead adders with a 240 ps 90 nm CMOS design example, *IEEE J. Solid-State Circuits, vol. 44,* no. 2, pp. 569–583, Feb. 2009.

[11] B. Ramkumar and H. M. Kittur, Low-power and area-efficient carry select adder, *IEEE Trans. Very Large Scale Integr. (VLSI) Syst., vol. 20,* no. 2, pp. 371–375, Feb. 2012.