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High Speed Implementation of 16 x 16 Multiplier Using Vedic Mathematics – A Review

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Abstract *– Extremely economical arithmetic operations are necessary to understand the required performance in many periods of time systems and digital image methodology applications. Vedic arithmetic is that the normal system of arithmetic that features a novel technique of calculations supported sixteen Sutras that are discovered by Sri Bharti Krishna Tirthaji. Throughout this work, the planned number style supported the sutra- 'Urdhva Tiryakbhyam' of Vedic arithmetic is analyzed and additionally the performance results of the amount are compared with standard multipliers.*

Keywords*: Vedic multiplier, Array Multiplier, Vedic Mathematics, Urdhva-Tiryagbhyam.*

I. Introduction

Multiplication is a very important basic arithmetic operation in Digital Signal processing (DSP) applications like Convolution, fast Fourier transform (FFT) and additionally in microprocessors [1, 2].Depending on the time consuming for the multiplication method we will confirm the performance of the system that uses number. So as to decrease the consumption of time we tend to need a high speed efficient number.

The design depends on the vertical and crosswise algorithm of ancient Indian Vedic arithmetic. That the performance of the number could also be a key element in crucial the presentation of the whole system. This could be because; the number is that the slowest and most time intense considers the system. That the optimization of the multiplier factor speeds and area is also a most important challenge for the structure designers. In his challenge is additionally successfully overcome by the use of ancient Vedic arithmetic. Vedic arithmetic is one among the foremost ancient methodologies utilized by the Aryans thus on perform mathematical computation [2].

The number style depends on the Vertical and Crosswise algorithm of antique Indian Vedic arithmetic. Many Digital signal processing (DSP) systems includes multipliers conjointly of core hardware blocks. Multipliers hold a significant role in various DSP applications like digital filtering; electronic communication and fast Fourier transform [4]. The common classification of multipliers betting on their style involves three types: 'serial multipliers', 'parallel multipliers' and 'serial-parallel multipliers'. Throughout this work, number style supported Urdhva tiryakbhyam sanskrit literature [6], an idea supported vedic arithmetic is mentioned.

Minimizing power consumption and delay for digital systems involves optimization at all levels of the planning. This optimization suggests that choosing the optimum algorithmic rule for the situation, this being the very best level of style, then the circuit style, the topology and at last the technology wont to implement the digital circuits. Depending upon the arrangement of the elements, there are differing kinds of multipliers offered. Particular multiplier design is chosen supported the application. Strategies of multiplication are documented within the Egyptian, Greek, Babylonian, Indus valley and Chinese civilizations.[1] In early days of Computers, multiplication was implemented usually with a sequence of addition, subtraction and shift operations. There exist several algorithms planned in literature to perform multiplication, every providing different benefits and having trade off in terms of delay, circuit complexity, area occupied on chip and power consumption.

They are four sorts of ancient arithmetic, the Vedas and vedic arithmetic is one in all part the four Vedas. The Atharva veda may be a UPA-Veda (appendix), the Sthapatya-Veda (Civil engineering and construction of the book), and a part of the atharva veda. Arithmetic, trigonometry geometry (plane, coordinate), quadratic equations, calculus issue, and conjointly as well as the description applies to several modern mathematical terms are explained during this atharva veda [6].

The word "Vedic" comes from the Sanskrit word "veda" which suggests the wisdom. The branches of maths like geometry, arithmetic, algebra, etc are solved

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His Holiness jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884 −1960 comprised all this work together and gave its mathematical explanation while using it for various applications. After thorough research in Atharva Veda, swahij described 16 sutras (formulae) and 16 upa sutras (sub formulas). In present text of Atharva Veda these formulae are not found because these formulae were implemented by Swamiji himself [6]. Vedic mathematics is a mathematical miracle, but it is also logically. That is the reason why Vedic mathematics has such a degree of fame. Because of this unusual characteristic, Vedic mathematics has already crossed the boundaries of India and became the upcoming topic of research. Several basic and complex multiplications can be easily solved by Vedic mathematic.They are many basic methods in vedic mathematics for arithmetic, which are very simple and effective.

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II. Literature Survey

S.P.Pohokar et. al[1] "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics" in this paper Vedic multiplier is efficient than Array multiplier. Because the variety of bit will increase from 8 x 8 bit to 16 x 16 bit, the timing delay greatly reduces for Vedic multiplier as compared to array multiplier. The time delay in vedic multiplier for 16 x 16 bit variety is 28.779 ns whereas the time delay for Array multiplier is 61.241 ns severally. The memory needed for 16 x 16 bit vedic multiplier is 169924 kilobytes and Array multiplier needed 178492 kilobytes. So vedic multiplier shows the improved speed among the standard multiplier and it additionally reduces the memory of the system. In future, this work might be extended to style and implement of Digital filters like FIR, IIR and frequency domain transformations like FFT and DCT algorithms.

Murugesan G. et al. [2] "Design and Implementation of High Speed Multiplier Using Vedic Mathematics", 16 x16 high speed multiplier is built, that is extremely efficient. The multiplier design relies on Urdhva-Tiryakbhyam sutra of vedic arithmetic and accumulation is done using adder, which provides higher performance when compared with different multipliers like Booth, Array and Wallace Tree multipliers. With this planned style, it's found that our style works with a lot of less delay of 22.201 ns. As a future improvement method, compressors or adders like carry save adder may be aggregate to the planned vedic number so the delay are often still a lot of reduced thereby increasing the speed. This additionally leads to reduction of logic levels to a large extent.

Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja et. al. [3] "Vedic arithmetic or Sixteen easy Mathematicle Formulae from the Veda", the utilization of Vedic arithmetic lies among the undeniable fact that it reduces normal|the quality} calculation among the quality arithmetic to very easy once. This can be therefore as a results of the vedic formulae have claimed to be building on the natural principles on it the human mind works. vedic arithmetic is additionally a several effective algorithms that has cowl to varied branches of engineering like computing. Throughout this work, I even have studied totally completely different multipliers, which supply low power demand and high speed, together supply data of "urdhva-Tiryabhyam" algorithm of ancient Indian vedic arithmetic, that has used for multiplication to strengthen speed, area parameters of multipliers.

Sudeep. et. al. [4] "Design and FPGA Implementation of High Speed Vedic Multiplier", Multiplication is an operation abundant needed in Digital Signal technique for varied applications. This paper puts forward a high speed vedic multiplier that's economical in terms of speed, making use of Urdhva Tiryagbhyam, a literature from vedic maths for multiplication and Kogge Stone formula for humanities addition of partial product and additionally compares it with the characteristics of existing several algorithms.

Shri Prakash Dwivedi et al. [5] "An Efficient Multiplication Algorithm Using Nikhilam Method," Multiplication is one in all the most necessary operations in pc arithmetic. several number operations like squaring, division and computing reciprocal need same order of time as multiplication whereas another operations like computing GCD and residue operation need at the most an element of log n time over multiplication. we tend to propose an number multiplication formula using Nikhilam technique of vedic arithmetic which might be used to multiply 2 binary numbers with efficiency.

G.Vaithiyanathan, et. al. [6] "Simulation and Implementation of Vedic multiplier factor exploitation VHDL Code" throughout a typical processor, Multiplication is one in each of the essential arithmetic operations and it desires well a great deal of hardware resources and amount than addition and subtraction. In detail, 8.72% of all the instruction in typical technique units is multipliers. In computers, a typical central

method unit devotes a substantial amount of sometime interval in implementing arithmetic operations, significantly multiplication operations.

Manoranjan Pradhan et. al [7] "Speed Comparison of 16x16 Vedic Multipliers", in this paper provides the extends multiplication to 16×16 Vedic multiplier factor exploitation "Nikhilam Sutra" technique. The 16×16 Vedic multiplier factor half victimization Urdhva Tiryagbhyam Sanskrit literature uses four 8×8 Vedic multiplier factor modules; one 16 bit carry save adders, and two 17 bit full adder stages. The carry save adder within the multiplier factor design will increase the speed of addition of partial product.

G.Ganesh Kumar, et. al. [8] "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques" it provides the planning of high speed Vedic number exploitation the techniques of Ancient Indian Vedic arithmetic that are customised to induce higher performance. Vedic arithmetic is that the ancient system of arithmetic that includes a distinctive technique of calculations supported sixteen Sutras.

III. Method

III.1. Vedic Multiplication

The Vedic multiplier is based on the Vedic multiplication formulae (Sutras). These Sutras have been traditionally used for the multiplication of two numbers in the decimal number system. In this work, we apply the same ideas to the binary number system to make the proposed algorithm compatible with the digital hardware. Vedic multiplication based on some algorithms, is discussed below:

A. Urdhva Tiryakbhyam sutra

The multiplier relies on AN algorithmic rule Urdhva Tiryakbhyam (Vertical & Crosswise) of ancient Indian vedic arithmetic. Urdhva Tiryakbhyam Sanskrit literature could be a general multiplication formula applicable to all cases of multiplication. It virtually suggests that "Vertically and crosswise". it's supported a unique conception through that the generation of all partial products will be done so, coincident addition of those partial products will be done. so parallelism in generation of partial products and their summation is obtained using Urdhava Tiryakbhyam. The algorithmic rule will be generalized for n x n bit variety. Since the partial products and their sums are calculated in parallel, the number is independent of the clock frequency of the processor. so the number will require identical amount of your time to calculate the product and thus is independent of the clock frequency. the net advantage is that it reduces the requirement of microprocessors to work at more and more high clock frequencies. Whereas the next clock frequency typically results in increased process power, its disadvantage is that it also will increase power dissipation which ends in higher device operating temperatures. By adopting the vedic number, microprocessors designers will simply circumvent these issues to avoid catastrophic device failures. The process power of number will simply be increased by increasing the input and output information bus widths since it's a quite a regular structure. Because of its regular structure, it will be simply layout during a silicon chip. The number has the advantage that because the variety of bits will increase, gate delay and space increases terribly slowly as compared to different multipliers. thus it's time, area and power efficient. it's demonstrated that this design is sort of efficient in terms of silicon area/speed.

B. Nikhilam Sutra

Nikhilam sutra virtually suggests that "all from 9 and last from 10". though it's applicable to all or any cases of multiplication, it's additional efficient once the numbers involved are massive. Since it finds out the compliment of the massive variety from its nearest base to perform the multiplication operation on that, larger is that the original variety, lesser the quality of the multiplication. We tend to 1st illustrate this sutra by considering the multiplication of 2 decimal numbers (96 * 93) in Fig 1. Wherever the chosen base is 100 that is nearest to and larger than each these 2 numbers.

The right hand aspect (RHS) of the product will be obtained by simply multiplying the numbers of the Column two (7*4 = 28). The hand side (LHS) of the product will be found by cross subtracting the second variety of Column two from the primary variety of Column one or vice versa, i.e., 96 - 7 = 89 or 93 - 4 = 89. The ultimate result's obtained by concatenating RHS and LHS (Answer = 8928).

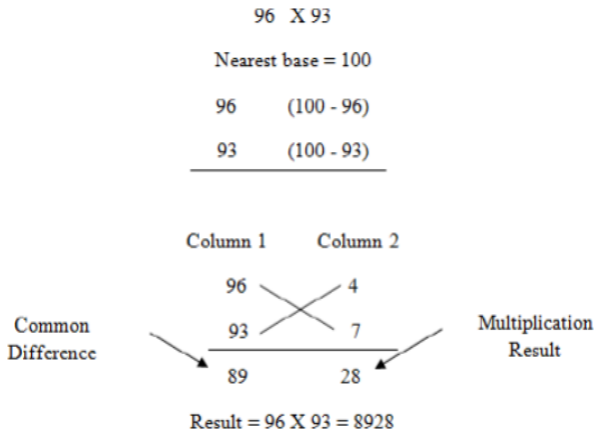

Fig.1 Multiplication Using Nikhilam Sutra

IV. Conclusion

In this paper, study of High Speed Implementation of 16 x 16 multiplier factor exploitation Vedic arithmetic. the multiplier factor is accomplished by instantiating the lower order bit multipliers like 8x8. This can be primarily because of memory constraints. Because of

factors of temporal order potency, speed, lesser space, the planned Vedic parallel overlay design is enforced in Arithmetic and Logical Units substitution the normal number design. . Effective memory implementation and deployment of memory compression algorithms can yield even better results in terms of area and speed which improves the overall performance of the design. Nikhilam Sutra based Vedic multiplier with BEC is highly efficient algorithm for multiplication.

References

[1.] S.P.Pohokar, R.S.Sisal, K.M.Gaikwad, M.M.Patil, Rushikesh Borse "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics" International Conference on Industrial Instrumentation and Control (ICIC)College of Engineering Pune, India. May 28-30, 2015

[2.] Sudeep. M. C, Sharath Bimba. M, Mahendra Vucha, "Design and FPGA Implementation of High Speed Vedic Multiplier", International Journal of Computer Applications, Volume 90-No. 16, March 2014.

[3.] G.Vaithiyanathan, K.Venkatesan, S.Sivaramakrishnan, S.Siva, and S. Jayakumar, "Simulation and Implementation of Vedic Multiplier Using VHDL Code" International Journal of Scientific & Engineering Research Volume 4, January-2013

[4.] R.Sridevi, Anirudh Palakurthi, Akhila Sadhula, Hafsa Mahreen,"Design of High Speed Multiplier(Ancient Vedic Mathematics Approach)", Internationan Journal of Engineering Research, Volume No.2,pp:183-186, July 2013.

[5.] Chilton Fernandes, Samarth Borkar, "Application of Vedic Mathematics in Computer Architecture", International Journal of Research in Engineering and Science (IJRES), Volume 1, September 2013.

[6.] Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja,"Vedic Mathematics or Sixteen Simple Mathematicle Formulae from the Veda, Delhi(1965)", Motilal Banarsidass, Varanasi,India.

[7.] C. Sheshavali, K. Niranjan Kumar, "Design and Implementation of Vedic Multiplier", International Journal of Engineering Research and Development, Volume-8, PP.23-28, September 2013.

[8.] Premananda B.S.Samarth S.Pai, ShashankB.,"Design and Implementation of 8-Bit Vedic Multiplier", International Journal of Advanced Research in Electrical, Electronics and Instrumentation Engineering, Volume 2, December 2013.

[9.] G.Ganesh Kumar, V.Charishma, "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques" International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012.

[10.] Manoranjan Pradhan, Rutuparna Panda, Sushanta Kumar Sahu, "Speed Comparison of 16x16 Vedic Multpliers", International Journal of Computer Applications, Volume 21-No.6, May 2011.

[11.] H. S. Dhillon and A. Mitra,"A Digital Multiplier Architecture using Urdhava Tiryabhyam Sutra of Vedic Mathematics", IEEE Conference Proceeding, 2008.

[12.] Purushottam D. Chidgupkar Mangesh T. Karad,"The Implementation of Vedic Algorithms in Digital Signal Processing" Global J. of Engng. Educ., Vol.8, No.

[13]. Sung-Mo Kang and Yusuf Leblebici, "CMOS digital integrated circuitsanalysisand design", third edition, Tata McGraw-Hill education Pvt.Ltd.

[14]. SuryasnataTripathy, L B Omprakash, B. S. Patro, Sushant K. Mandal, "A comparative analysis of different 8-bit adder topologies at 45 nm technology", International journal of engineering research andtechnology, vol. 2, Issue 10, October 2013.

[15]. SuryasnataTripathy, L B Omprakash, B. S. Patro, Sushanta K. Mandal, "Low power, high speed full adder architectures in 45nm technology", International conference on VLSI and signal processing, IIT Kharagpur, Jan 10-12, 2014.

[16.] Manoranjan Pradhan, Rutuparna Panda, Sushanta Kumar Sahu, "Speed Comparison of 16x16 Vedic Multpliers", International Journal of Computer Applications, Volume 21-No.6, May 2011.

[17.] H. S. Dhillon and A. Mitra,"A Digital Multiplier Architecture using Urdhava Tiryabhyam Sutra of Vedic Mathematics", IEEE Conference Proceeding, 2008.

[18.] Purushottam D. Chidgupkar Mangesh T. Karad,"The Implementation of Vedic Algorithms in Digital Signal Processing" Global J. of Engng. Educ., Vol.8, No.

[19]. Sung-Mo Kang and Yusuf Leblebici, "CMOS digital integrated circuitsanalysisand design", third edition, Tata McGraw-Hill education Pvt.Ltd.

[20]. SuryasnataTripathy, L B Omprakash, B. S. Patro, Sushant K. Mandal, "A comparative analysis of different 8-bit adder topologies at 45 nm technology", International journal of engineering research andtechnology, vol. 2, Issue 10, October 2013.

[21]. SuryasnataTripathy, L B Omprakash, B. S. Patro, Sushanta K. Mandal, "Low power, high speed full adder architectures in 45nm technology", International conference on VLSI and signal processing, IIT Kharagpur, Jan 10-12, 2014.

[22]. D. Radhakrishnan, "Low-voltage low-power CMOS full adder", Proc. Inst. Elect. Eng., Circuitts Devices and Systems, vol. 148, no. 1, pp. 19- 24, 2001.

[23]. Deepa Sinha, Tripti Sharma, K.G.Sharma, Prof.B.P.Singh, " Design and analysis of low power 1 bit full adder cell", IEEE 3rd International Conference on Electronics Computer Technology (ICECT) , vol.2, pp.303-305, 8-10 April 2011.

[24]. SuryasnataTripathy, Sushanta K. Mandal, " High speed low power datapath design using multi threshold logi c in 45 nm technology for signal processing application", National Conference on VLSI Signal Processing and Trends in Telecommunication (VSATT-2014), C V Raman College of Engineering, Odisha, May 9-10, 2014.

[25]. Youn Sang Lee, JeongBeom Kim, "Design of a low power 8×8 bit parallel multiplier using Mos current mode logic circuit ", IEEE proceedings on 8th international conference on solid state and integrated circuit technology, 2006, pp 1502-1504.

[26]. Swami BharatiKrshnaTirthaji, Vedic Mathematics. Delhi: MotilalBanarsidass Publishers, 1965.

[27]. K.K.Parhi "VLSI Digital Signal Processing Systems -Design and Implementation" John Wiley & Sons, 1999.

[28]. Harpreet Singh Dhillon and Abhijit Mitra "A Digital Multiplier Architecture using Urdhava Tiryakbhyam Sutra oj Vedic Mathematics" IEEE Conference Proceedings, 200S.

ISSN: 2274-1412

[29]. AsmitaHaveliya "A Novel Design ./i)r High Speed Multiplier .fir Digital Signal Processing Applications (Ancient Indian Vedic mathematics approach)" International Journal of Technology And Engineering System (IJTES):Jan - March 2011- Vo12 .Nol.3

[30.] G.Ganesh Kumar, V.Charishma, "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques" International Journal of Scientific and Research Publications, Volume 2, Issue 3, March 2012.