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High Speed Integration in DDR3 Controller

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Abstract *– The required for high speed and small size memories has been accelerating by the day. All device size diminishes gradually in electronics industry, for the perfect handing and carrying. Hence, these memory devices are quickly developing to provide high density and high memory bandwidths. Therefore, with the increase in technology, complication of commands to command the memory devices also accelerates. This paper, purpose influence speed and reduce power in DDR3 Controller. This paper represents the technique and architecture of the DDR3 Controller which utilizes to influence the speed and discuss advantages of DDR3.*

Keywords*: Optimized DDR3; Verilog; Xilinx; FPG, .High Speed DDR3*

I. Introduction

The DDR3 SDRAM utilizes an appropriate architecture to obtain high speed operation. The differential data strobe (DQS, DQS#) is communicated externally, along accompanied by data, for utilization in record at the DDR3 SDRAM input receiver. In computing systems, DDR3 SDRAM or double data rate three synchronous dynamic random access memory is a technology utilized for high bandwidth deposition of the adequate data of a computer or other digital electronic devices. DDR3 is portion of the SDRAM family of technologies and is one of the several DRAM (dynamic random access memory) executions.

The primary profit of DDR3 is the capability to transfer I/O data at eight times the data rate of the memory cells it consists, thus enabling higher bus rates and higher peak rates as comparison to earlier memory technologies. However, there is no associating decrease in latency, which is therefore proportionally higher. In addition to this, the DDR3 specific permits for chip capacities of 512 megabits to 8 gigabits, beneficially enabling a maximum memory module formulation of 16 gigabytes. However, going with the recent tradition of increasing memory demands, we required RAM which is faster, better and has additional capacity. According to this point of view, we have concluded to represent DDR4 SDRAM controller. Read and write accesses to the DDR3 SDRAM are burst-oriented. An access initializes at a pre-defined location and synchronizes for a programmed number of locations in a programmed arrangement. Accesses begin with the registration of ACTIVATE command which is followed by a READ or WRITE command. The address bits registered simultaneous with the ACTIVATE command are utilized to choose the bank and row to be accessed. The structure of DDR3 SDRAM permits pipelining along with self-refresh mode, power saving and power down mode.

II. Literature Rewiew

The Xin Yang, Sakir Sezer, John McCanny, Dwayne Burns (DDR3 BASED LOOKUP CIRCUIT FOR HIGH-PERFORMANCE NETWORK PROCESSING), in this paper, a modified DDR3 memory controller structure for high-performance table lookup is introduced and its deployment under a high-performance Hash-CAM based lockup circuit is presented. The design study has visualize that high-performance and large lookup table circuits can be executed by utilizing low-cost state-of-the-art FPGA and DDR3 technology. The introduced DDR3 Hash-CAM circuit is prototyped for a 128K table entry and substantiates for a 2Gbyte DDR3 address space. Synthesis outputs presented in Table I show that a CAM circuit accompanied by the 104bit range and 512-entry can be built on specific FPGA devices at 100MHz, operating frequency. Considering such an embedded CAM sub-circuit and a 2Gbyte DDR3 module, the introduced DDR3 Hash-CAM lookup architecture is capable of supporting 104bit range and 1M-entrant TCP/IP header lookup table with a sustainable lookup

behavior of up to 100 million packets per second. Considering a worst condition smallest packet size of 64bytes, the introduced lookup circuit is satisfactory for router or switch ports for location lookup or packet classification at sustainable line-rates above 50Gbit/s.

K.SIREESHA, S.UPENDER (Design of High Speed DDR3 SDRAM Controller), in this paper, an modified DDR3SDRAM controller structure was represented and which is able interface accompanied by a high performance Hash-CAM dependent lockup circuit. The DDR3SDRAM controller simple write, read and quick read operations are corrected by simulation and DDR3SDRAM controller is synthesized. Under this work, the DDR3SDRAM controller is represented and it can interface accompanied by the Look up table depend on Hash CAM circuit. CAM is generated to find its overall memory in a single operation; it is much quicker than RAM in virtually all search applications. The structure of DDR3SDRAM controller involves Initialization fsm Command fsm, data path , bank control ,clock counter, refresh counter, Address FIFO, instruction FIFO ,Wdata FIFO and R_data reg.

Shabana Aqueel and Kavita Khare (Design and FPGA Implementation of DDR3 SDRAM Controller for High Performance), in this paper designed a high speed DDR3 SDRAM Controller utilizing Micron's DDR3 memory model (MT41J128M8). The controller is written in VHDL language. The tool utilized to synthesize it and verify is Xilinx. A complete task file containing all operations was fixed up. Then, all technique registers were initialized. Finally, test bench with various test conditions were set up to correct the assumed results Number of Slices: 210 out of 768 27%, Number of Slice Flip Flops: 304 out of 1536 19%, Number of 4 input LUTs : 263 out of 1536 17%.

M.Rajendra, N.Suresh Babu (Speed and Area optimized Design of DDR3 SDRAM(Double Data Rate3 Synchronously Dynamic RAM) Controller for Digital TV Decoders), Under this paper author have designed a High speed DDR3 SDRAM Controller accompanied by the 64-bit data transfer which synchronizes the transfer of data among DDR RAM and External peripheral devices such as host computer, laptops and so on. The advantages of this controller as compared to SDR SDRAM DDR1 SDRAM and DDR2SDRAM is that it synchronizes the data transfer, and the data transfer is twice as fast as earlier, the production cost is also very less. When compare with the existing one the introduced design absorbs less area and high speed due to efficient design of the finite state machine.Author have designed using Verilog HDL and simulated utilizing Modelsim and synthesized utilizing Xilinx tool.

III. Proposed Modification

The frequencies of DDR4 memory could be increased beyond those of DDR3 due to doubling of the data prefetch that was transmitted from the info storage device to the input or output buffer. While DDR3 SDRAM utilizes 8-bit samples, DDR4 SDRAM utilizes 12-bit prefetch also termed as 12n-prefetch. In other words, DDR4 SDRAM technology implicit increase of the internal bus range among the real DRAM core and the input or output buffer. As a result of this, the increase in the efficient data transfer rate offered by DDR4 SDRAM doesn't need quick operation of the memory core. Only external buffers begin working quicker. As for the core frequency of the memory chips, it appears 8 times less than that of the external memory bus and DDR4 buffers (this frequency was 4 times lower than that of the external bus by DDR2) So, DDR4 memory can almost instantly hit higher true frequencies than DDR2 and DDR3.SDRAM, without any modifications or improvements of the semiconductor manufacturing processes. However, the above explained technique also has another side to it: unfortunately, it increases not only memory bandwidth, but also memory latencies. As a result, we shouldn't always imagine DDR3 SDRAM to work quicker than DDR2 SDRAM, even if it operates at higher frequencies than DDR2.

In our project, we have developed a high speed and less power DDR3 SDRAM controller taking every opportunity to decrease organization latencies while maintaining low power during peak read or write times. This was obtained through extremely dedicated hardware space explorations which enabled to optimize the speed of the controlling FSM to a great extent.

We introduced arbiter block for the design High speed DDR3 SDRAM.

IV. Arbiter Block

The organizations are attached to arbiter block modules which contain all the important FIFOs for buffering read and write commands and data ahead they are transmitted between the system and the memory controller. The FIFOs that are enclosed in the arbiter block, consist of two address FIFOs utilized for buffering the locations for either write or read instructions, a 64-to-512 write data FIFO utilized for buffering write data that is to be transferred from system to the memory, and 512-to-64 read data FIFO utilized for buffering read-back data among the memory controller and the system. Write data (wd_fifo), write address (wa_fifo) and read address (ra_fifo) FIFOs are impregnate at system clock's frequency, and discharged at memory controller clock's frequency.

V. Conclusion

This paper introduced high speed area well organized DDR3SDRAM, which is represent in Xilinx software accompanied by the support of VERILOG code. Proposed to represent ddr4sdram by design high prefetch cycle and correction of buffer data. We synchronize FSM with FIFO for high speed and low power.

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