International Journal of advancement in electronics and computer engineering (IJAECE)
Volume 3, Issue 8, November 2014, pp.351-354, ***ISSN 2278 -1412***

Speed Enhancement In DDR3 SDRAM Using FIFO Synchronization Technique

VinusTyagi[1], Rahul Shrivastava[2], Rita Jain[3]

Department of Electronics & Telecommunication, LNCT, Bhopal, India
[1]vinus009@gmail.com, [2]rahul.stva@gmail.com, [3]ritajain_bpl@gmail.com

Abstract-*The demand for high speed and small size memories has been increasing by the day. All device size is decreasing day-by-day in electronics industry for the best handing and carrying. Hence, these memory devices are rapidly developing to give high density and high memory bandwidths. However, with the increase in technology, complexity of instructions to control the memory devices also increases. This paper presents the technique and architecture of the DDR3 Controller which can be used to enhance the speed and discuss advantages of DDR3.*

Keywords: *Double Data Rate(DDR), First-In First-Out (FIFO), Field Programmable Gate Array(FPGA), Finite State Machine(FSM), Input-Output(I/O), Integrated Software Environment(ISE), Static Dynamic Random Access Memory(SDRAM), Look-Up-Table(LUT), Random Access Memory(RAM).*

I. Introduction

The DDR3 SDRAM uses an 8n prefetch architecture to achieve high speed operation. In computing systems, DDR3 SDRAM or double data rate three synchronous dynamic random access memory is a technology used for high bandwidth storage of the working data of a computer or other digital electronic devices. DDR3 is part of the SDRAM family of technologies and is one of the many DRAM (dynamic random access memory) implementations.

The primary benefit of DDR3 is the ability to transfer I/O data at eight times the data rate of the memory cells it contains, thus enabling higher bus rates and higher peak rates than earlier memory technologies. However, there is no corresponding reduction in latency, which is therefore proportionally higher. In addition, the DDR3 standard allows for chip capacities of 512 megabits to 8 gigabits, effectively enabling a maximum memory module size of 16 gigabytes. However, going with the present trend of increasing memory requirements, we need RAM which is faster, better and has more capacity. In view of this, we have decided to design DDR4 SDRAM controller.

The associated interface techniques used by DDR3 SDRAM is not directly compatible with any earlier type of random access memory (RAM) due to different signaling voltages, timings, and other factors. With two transfers per cycle of a quadrupled clock, a 64-bit wide DDR3 module may achieve a transfer rate of up to 64 times the memory clock speed in megabytes per second (MB/s). In addition, the DDR3 standard permits chip capacities of up to 8 gigabits. The primary benefit of DDR3 SDRAM over its immediate predecessor, DDR2 SDRAM, is its ability to transfer data at twice the rate (eight times the speed of its internal memory arrays), enabling higher bandwidth or peak data rates.

II. Top Module

The top module of the DDR3 SDRAM Controller is shown in Figure 1. It consists of 3 modules, the main controller module, the signal module and the data path module. The user sends the data to be written onto or read from the DDR3 SDRAM along with the memory location (address). The main controller module has two state machines and a refresh counter. The signal generation module generates the address and command signals required for DDR3. The data path module performs the data latching and dispatching of the data between the processor and DDR3.

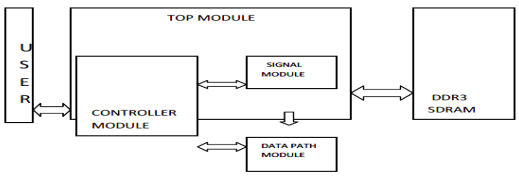

Fig.1 Block Diagram of Top Module

III. DDR3 Features Comparison

DDR3 is the next-generation, high-performance solution for CPU systems it pushes the envelope in key areas like power consumption, signaling speeds, and bandwidth, bringing new levels of performance to desktop, notebook, and server computing. DDR3 offers a substantial performance improvement over the previous DDR2 and DDR memory systems. One of the main DDR3 features include improved signal integrity so as to have higher performance without an undue burden on the system designer. Table.1 compares some differences between DDR3 and the previous two hierarchies.

TABLE I
Comparison of different DDR Features

FEATURES	*DDR1*	*DDR2*	*DDR3*
DATA RATE	200-400Mbps	400-800Mbps	800-1600Mbps
BURST LENGTH	BL=2,4,8	BL=4,8	BL=4,8
NO 0F BANKS	4 banks	512 MB : 4Banks 1 GB : 8Banks	512MB/1GB:8 Banks
PREFETCH	2Bit	4Bit	8Bit
Vdd/Vddq	2.5+/ -0.2V	1.8+/-0.1V	1.5+/0.075V

IV. DDR3 SDRAM

DDR3 provides two burst modes for both reading and writing: burst chop (BC4) and burst length eight (BL8). BC4 allows bursts of four by treating data as though half of it is masked. This creates smooth transitioning if switching from DDR2 to DDR3 memory.

However, burst mode BL8 is the primary burst mode. BL8 allows the most data to be transferred in the least amount of time; it transfers the greatest number of 64-bit data packets (eight) to or from consecutive addresses in memory, which means addressing occurs once for every eight data packets sent. In order to support a burst length of eight data packets, DDR3 SDRAM has an 8-bit prefetch buffer.

The frequencies of DDR3 memory could be raised beyond those of DDR2 due to doubling of the data prefetch that was moved from the info storage device to the input/output buffer. While DDR2 SDRAM uses 4-bit samples, DDR3 SDRAM uses 8-bit prefetch also known as 8n-prefetch.

In other words, DDR3 SDRAM technology implies doubling of the internal bus width between the actual DRAM core and the input/output buffer. The main controller module has two state machines and a refresh counter. The signal generation module generates the address and command signals required for DDR3.

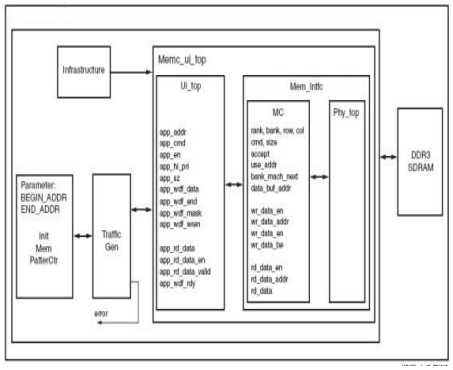

Fig.2. Block diagram of proposed design

V. Design of DDR3 SDRAM Controller

Before normal memory access can be performed DDR3 SDRAM should be initialized first. So, the controller block consists of FSMs (Finite state machines) with FIFO, One is the initialization FSM and the other is the command FSM. The initialization involves the predefined steps described in FSM Algorithm. The command FSM handles the read, write and refresh of DDR3. The initialization FSM consists of all the possible states to be encountered during initialization. Once the initialization is done the DDR3 SDRAM is ready for either writing data into or reading data from its store. Read write function working in FIFO mode. The command FSM mainly contains two states READ and WRITE state, besides, continuous REFRESH state (as it's a dynamic RAM). When either of the states are met a sequence of internal signals are generated corresponding to that state.

V.1. Memory controller Block

The memory controller module came with the original Xilinx example design project which our design was leveraged on. It is used to simplify communication to the memory by taking care of the refresh cycle, and enabling the system to use a simple BL8 interface. In BL8 mode every address is associated with 512 bit data packets, which creates a need for the arbiter design to have some sort of serial-to- parallel converter so that it would map to a reasonable number of physical pins.

V.2. Arbiter block

The systems are connected to arbiter_block modules which consist of all necessary FIFOs for buffering read and write commands and data before they are transferred between the system and the memory controller. The FIFOs that are encapsulated in the arbiter_block, include two address FIFOs used for buffering the addresses for either write or read commands, a 64-to-512 write data FIFO used for buffering write data that is to be sent from system to the memory, and 512-to-64 read data FIFO used for buffering read-back data between the memory

controller and the system. Write data (wd_fifo), write address (wa_fifo) and read address (ra_fifo) FIFOs are filled at system clock's frequency, and emptied at memory controller clock's frequency. Read-back data FIFO is filled at memory controller clock's frequency and emptied at system clock's frequency. The reading and writing to these FIFOs is controlled in mostly controller by the state-machine in the arbiter block that is shown inFigure.

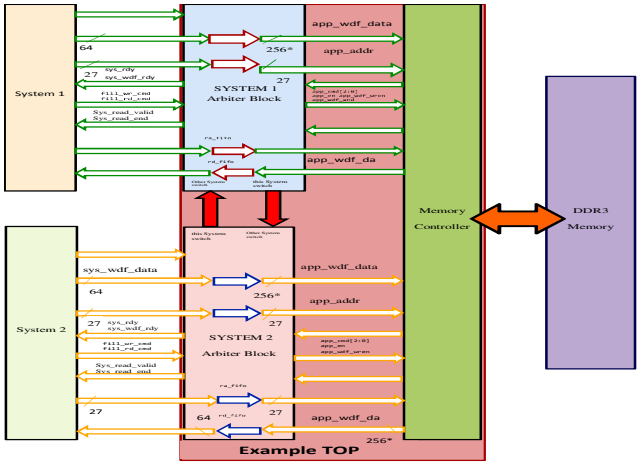

Fig.3 Two arbiter blocks set-up to connect the DDR3 memory to two different systems

VI. Simulation Result

In this work we have designed a high speed DDR3 SDRAM. The code is written in VERILOG language. The tool used to synthesize it and verify is Xilinx. A complete task file including all operations was set up. Then, all mode registers were initialized. Finally, test bench with several test cases were set up to verify the expected results. The Figure shows the RTL schematic of the top module and the controller respectively.

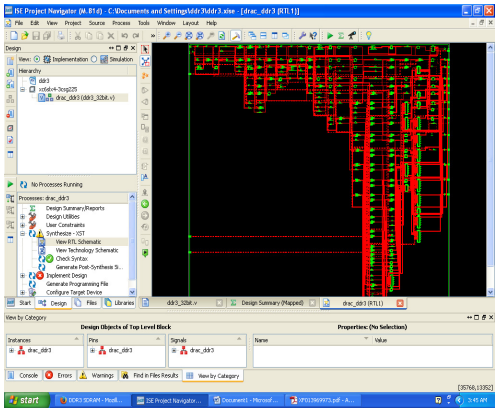

Fig.4 Technology view of the SDRAM controller

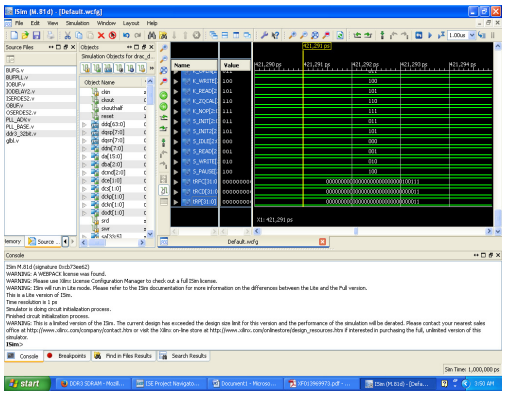

Fig.5 Simulation of the SDRAM controller

TABLE II

HDL Synthesis Report

Macro Statistics	
# Adders/Subtractors	: 4
11-bit adder	:1
14-bit adder	:2
6-bit subtractor	:1
# Registers	:49
1-bit register	:30
11-bit register	:1
14-bit register	:2
2-bit register	:3
256-bit register	:2
3-bit register	:4
32-bit register	:1
6-bit register	:1
64-bit register	:5
# Multiplexers	:79
1-bit 2-to-1 multiplexer	:47
11-bit 2-to-1 multiplexer	:1
2-bit 2-to-1 multiplexer	:4
3-bit 2-to-1 multiplexer	:14
6-bit 2-to-1 multiplexer	:5
64-bit 2-to-1 multiplexer	:8
Slice Logic Utilization	
Number of Slice Registers:	677 out of 4800 14%
Number of Slice LUTs:	370 out of 2400 15%
Number used as Logic:	369 out of 2400 15%
Number used as Memory:	1 out of 1200 0%
Number used as SRL:	1

Slice Logic Distribution	
Number of LUT Flip Flop pairs used:	702
Number with an unused Flip Flop:	25 out of 702 3%
Number with an unused LUT:	332 out of 702 47%
Number of fully used LUT-FF pairs:	345 out of 702 49%
Number of unique control sets:	23
Number of IOs:	711
Number of bonded IOBs:	711 out of 132 538% (*)
IOB Flip Flops/Latches:	288
Specific Feature Utilization	
Number of BUFG/BUFGCTRLs:	3 out of 16 18%
Number of PLL_ADVs:	1 out of 2 50%
Minimum period:	3.068ns
Maximum Frequency:	325.974MHz
Minimum input arrival time before clock:	4.143ns
Maximum output required time after clock:	6.161ns
Maximum combinational path delay:	3.150ns
Delay:	2.723ns (Levels of Logic = 1)

VII. Conclusion

This paper proposed high speed area efficient DDR3SDRAM, the architecture is evaluated in FPGA using Xilinx ISE Design Suite. In designing, the system using 14% of slice registers and 15% of slices LUTs. Thus, it occupies less area and consuming less power. This proposed system provides high speed operation because of synchronization FSM with FIFO.

Reference

[1] Xin Yang, SakirSezer, John McCanny, Dwanyne Burns, "DDR3 Based Look-up circuit for High Performance network Processing", IEEE 2009, pp 351-354.

[2] ShabanaAqueel and KavitaKhare, "Design and FPGA Implementation of DDR3 SDRAM Controller for High Performance", International Journal of Computer Science & Information Technology (IJCSIT) Vol 3, No 4, August 2011.

[3] DDR3 SDRAM Specification (JESD79-3A), JEDEC Standard, JEDEC Solid State Technology Association, Sept. 2007.

[4] "Double Data Rate (DDR3) IP Core User's Guide", Lattice Semiconductors Corporation, Dec.2010.

[5] "High-Performance DDR3 SDRAM Interface in Virtex-5 Devices", Xilinx, XAPP867 (v1.0), Sept 24, 2007.

[6] www.altera.com/literature/ug/ug_altmemphy.pdf, External DDR Memory PHY Interface Mega function User Guide (ALTMEMPHY), 23 Feb. 2009.

[7] Micron 1GB DDR3 SDRAM , Micron Technology Inc. , 2006.

[8] VikkyLakhmani, Nusrat Ali, Dr. Vijay Shankar Tripathi, "AXI Compliant DDR3 Controller", Second International Conference on Computer Modeling and Simulation, 2010, pp 391-395.

[9] J. Bhasker "A VHDL Primer", 3rd Edition ,Pearson Education.

[10] DDR3 Power-up, Initialization, and Reset, Technical Note, TN-41-07, Micron.