International Journal of advancement in electronics and computer engineering (IJAECE)
Volume 2, Issue 10, January 2014, pp.265-270, ***ISSN 2278 -1412***

Implementation of a Seven Level Multilevel Inverter

Shadma khan[1], Monika jain[2],

[1]*Mtech scholar, oriental college of science and technology Bhopal,khanshadma95@yahoo.in,india;*

[2]*Electrical & Electronics Department, Oriental college of Science & Technology Bhopal ,India;*

Abstract- Power-electronic inverters are becoming popular for various industrial drives applications. In recent years also high-power and medium-voltage drive applications have been installed. Performance of multilevel inverter is superior to that of two level inverters due to reduced harmonic distortion and reduced electromagnetic interference. But it has some disadvantages also such as increased number of components and voltage balancing. This paper describes the general multilevel inverter schematic. Seven level multilevel inverters consist of ten IGBT Switches and three carriers. The multilevel converter works only in positive polarity and does not generate negative polarities. In this paper we are measuring output voltage and Total Harmonic Distortion (THD).A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels.

Keywords: *SPWM, multilevel inverter, harmonic elimination*

I. Introduction

Multilevel inverters have been recently used in many industrial applications such as AC power supplies, drive systems, static VAR compensators etc.One of the advantage of multilevel inverter is harmonic reduction in the output waveform without increasing switching frequency .The output voltage waveform of a multilevel inverters is composed of number of levels of voltages [1].

The 2-level inverters have several problems with high frequency switching, which produce high voltage changes. Some other drawbacks are switching losses will be more, large dv/dt triggering, higher order harmonics etc.Because of these disadvantages of 2-level inverters, there is need to develop more efficient imverter.Multilevel inverters have many advantages as compared with 2-level inverter .the main features are less switching stress on devices, high voltage and high power capability, reduced dv/dt, good EMC, no need of extending the device rating.

The multilevel starts from three levels. As the number of levels reach infinity, the output THD (Total Harmonic Distortion) approaches zero. The number of the achievable voltage levels, however, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout, and packaging constraints. Multilevel inverters synthesizing a large number of levels have a lot of merits such as improved output waveform, a smaller filter size, a lower EMI (Electro Magnetic Interference), and other advantages. The principle advantage of using multilevel inverters is the low harmonic distortion obtained due to the multiple voltage levels at the output and reduced stresses on the switching devices used. There are many techniques, which are applied to multilevel inverter topologies. Pulse Width Modulation (PWM) is widely employed to control the output of static power inverters. The reason for using PWM is that they provide voltage and/or current wave shaping customized to the specific needs of the application under consideration. It is lastly performance and cost criteria which determines the choice of a PWM method in a specific application. PWM inverters can control their output voltage and frequency simultaneously. And also they can reduce the harmonic components in load currents. These features have made them power candidate in many industrial applications such as variable speed drives, uninterruptible power supplies, and other power conversion systems.

II. System configuration

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency wave-form in positive and negative

polarities. However, there is no need to utilize all the switches for generating bipolar levels.

This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named *level generation* part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability.

The other part is called *polarity generation* part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level genera-tion), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

The Reverse Voltage topology in seven levels is shown, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage in Fig. 1 generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage.

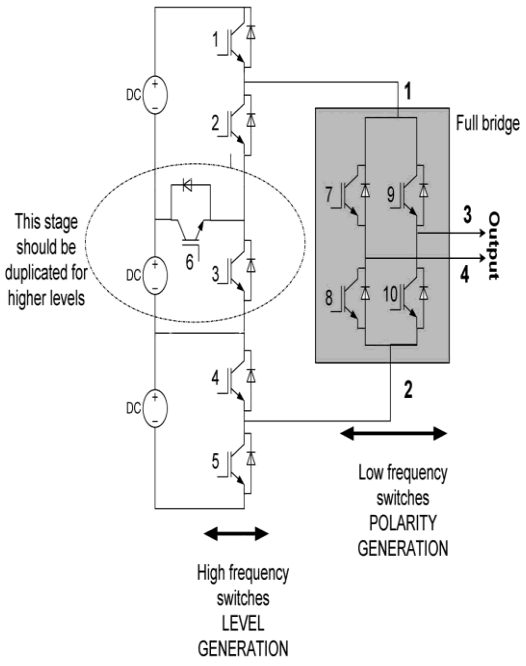

Fig.1 Schematic of a seven-level inverter in single phase

III. Multilevel topology

A new multilevel inverter topology named reversing voltage (RV). This topology requires less number of components compared to conventional topologies. It is also more efficient since the inverter has a component which operates the switching power devices at line frequency. Therefore, there is no need for all switches to work in high frequency which leads to simpler and more reliable control of the inverter.

This paper describes the general multilevel inverter schematic. A general method of multilevel modulation phase disposition (PD) SPWM is utilized to drive the inverter and can be extended to any number of voltage levels.

Recent advances in power electronics have made the multilevel concept practical. The concept is so advantageous that several major drives manufacturers have obtained recent patents on multilevel power converters and associated switching techniques. It is evident that the multilevel concept will be a prominent choice for power electronic systems in future years, especially for medium-voltage operation. Multi-level inverters are the modification of basic bridge inverters. They are normally connected in series to form stacks of level.

The topological structure of multilevel inverter must cope with the following points.

1. It should have less switching devices as far as possible.

2. It should be capable of enduring very high input voltage such as HVDC transmission for high power applications.

3. Each switching device should have lower switching frequency owing to multilevel approach.

There are various multilevel concepts used for various applications. Various multilevel circuits are used to generate multiple voltage levels. Some of the multilevel concepts with various voltage levels are given below multilevel inverters have been widely accepted for high-power high-voltage applications. Their performance is highly superior to that of conventional two-level inverters due to reduced harmonic distortion, lower electromagnetic interference, and higher dc link voltages. However, it has some disadvantages such as increased number of components, complex pulse width modulation control method, and voltage-balancing problem. A new topology with a reversing-voltage component is proposed to improve the multilevel performance by compensating the disadvantages mentioned. This topology requires fewer components compared to existing inverters (particularly in higher levels) and requires fewer carrier signals and gate

drives. There- fore, the overall cost and complexity are greatly reduced particularly for higher output voltage levels.

In conventional multilevel inverters, the power semiconductor switches are combined to produce a high-frequency wave- form in positive and negative polarities. However, there is no need to utilize all the switches for generating bipolar levels. This idea has been put into practice by the new topology.

This topology is a hybrid multilevel topology which separates the output voltage into two parts. One part is named level generation part and is responsible for level generating in positive polarity. This part requires high-frequency switches to generate the required levels. The switches in this part should have high-switching-frequency capability.

The other part is called polarity generation part and is responsible for generating the polarity of the output voltage, which is the low-frequency part operating at line frequency.

The topology combines the two parts (high frequency and low frequency) to generate the multilevel voltage output. In order to generate a complete multilevel output, the positive levels are generated by the high-frequency part (level generation), and then, this part is fed to a full-bridge inverter (polarity generation), which will generate the required polarity for the output. This will eliminate many of the semiconductor switches which were responsible to generate the output voltage levels in positive and negative polarities.

The RV topology in seven levels, it requires ten switches and three isolated sources. The principal idea of this topology as a multilevel inverter is that the left stage generates the required output levels (without polarity) and the right circuit (full-bridge converter) decides about the polarity of the output voltage. In order to produce seven levels by SPWM, three saw-tooth waveforms for carrier and a sinusoidal reference signal for modulator are required as shown.

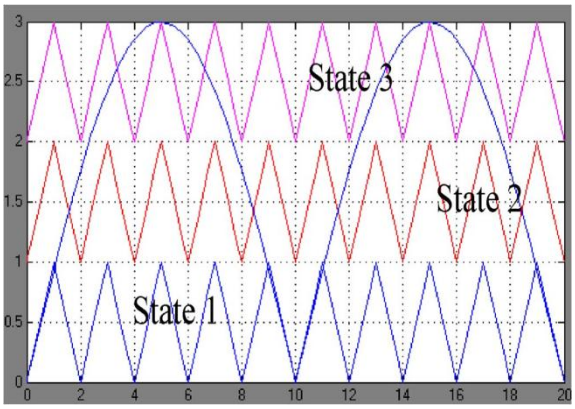

Fig.2 SPWM carrier and modulator for RV topology

Carriers in this method do not have any coincidence, and they have definite offset from each other. They are also in phase with each other. The Modulator and three Carriers for SPWM. According to Fig. 4.3, three states are considered. The first state is when the modulator signal is within the lowest carrier. The second state is when it is within the middle carrier. Finally, the third one is when it is within the highest carrier. In each state, certain switching patterns are adopted to cover the voltage requirements.

Therefore, the number of switches in the proposed topology that conduct the circuit current is lower than that of the cascade inverter, and hence, it has a better efficiency. The same calculation is true in a topology mentioned. The least number of switches in the current path for a seven level inverter according to is five (for generating level 3), which requires one switch more in the current path compared to the proposed topology which requires only four conducting switches.

These switching sequences can be implemented by logic gates or DSP. The signal stage should be isolated from the power stage by opt couplers for control circuit protection. The drive circuit is also responsible to generate the dead time between each successive switching cycle across the dc source.

The gating signal for the output stage, which changes the polarity of the voltage, is simple. Low-frequency output stage is an H-bridge inverter and works in two modes: forward and reverse modes. In the forward mode, switches 8 and 9 conduct, and the output voltage polarity is positive. However, switches 7 and 10 conduct in reverse mode, which will lead to negative voltage polarity in the output. Thus, the low-frequency polarity generation stage only determines the output polarity and is synchronous with the line frequency.

The resulting PWM waveforms for driving the high frequency switches in the level generation part are illustrated for one complete cycle in Fig.3 According to Fig.3, high frequency switches can be adopted in this stage based on the required frequency and voltage level. However, low-frequency polarity generation part drive signals are generated with the line frequency (50 Hz), and they only change at zero-voltage crossings

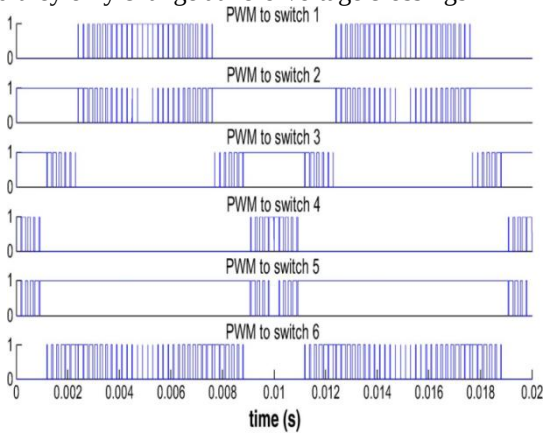

Fig. 3 Complete gate signals for level generation part

The proposed converter, as can be seen, half of the switches in the full-bridge converter will not require to be switched on rapidly since they are only switched at zero crossings operating at line frequency (50 Hz). Thus, in this case, the reliability of the converter and also related expenses are highly improved. It can with higher voltage levels. Fig. 4.6 shows the required components versus different voltage levels as mentioned. As the most important part in multilevel inverters is the power clearly be inferred that the number of components of the proposed topology is lower than that of other topologies even more so as the voltage levels increase and it will decrease tremendously semiconductor switches which define the reliability.

IV. Simulation results

Seven level conventional converters consist of ten IGBT Switches and three carriers. The multilevel converter works only in positive polarity and does not generate negative polarities. In this paper are measure output voltage and Total Harmonic Distortion (THD).

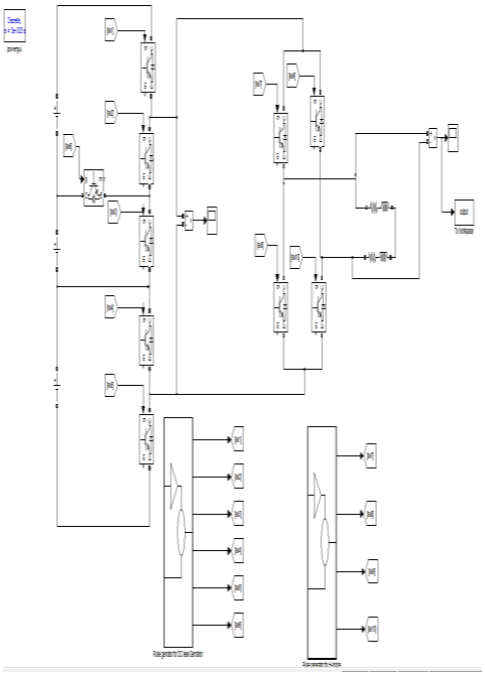

Fig.4Simulated model proposed seven level Inverter

The pulse is generated by comparison between Sine wave and Carrier waves. After using the logic gate operations we are getting required three more Pulses There is Sine wave used for generation the sinusoidal waveform. After this we are using gain (-1), which is used for getting the Positive Output voltage. And a Switch is used for the passing of signal. Pass through input one when satisfies input Two selected criteria, otherwise passed through input third. There are three carriers wave comparing to sinusoidal wave with the help of three repeating sequences. And after this we are using logic gate operations NOT, AND, OR, NOR. Then we got the six Output pulses.

Logic Operations:

Table I.

NOT Operation

Input	Output
0	1
1	0

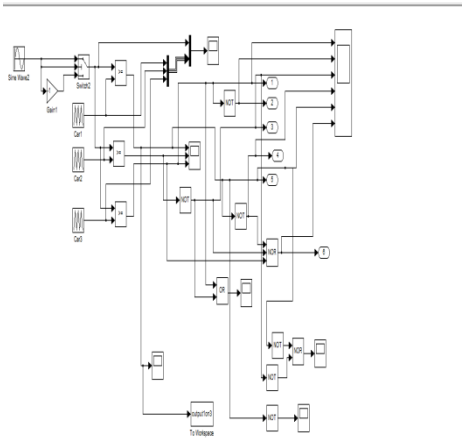

Fig.5 Simulink model of PWM block of the proposed seven level Inverter

V. Output Waveform of MLI

The Output waveform of DC Levels

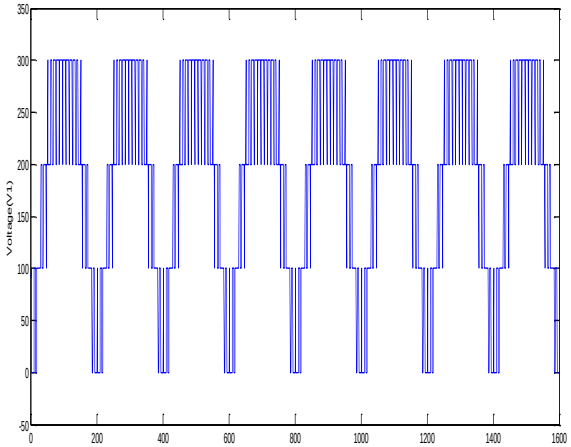

Fig.6 DC level waveform of seven levelInverter

This is the output voltage waveform of the Seven level Inverter

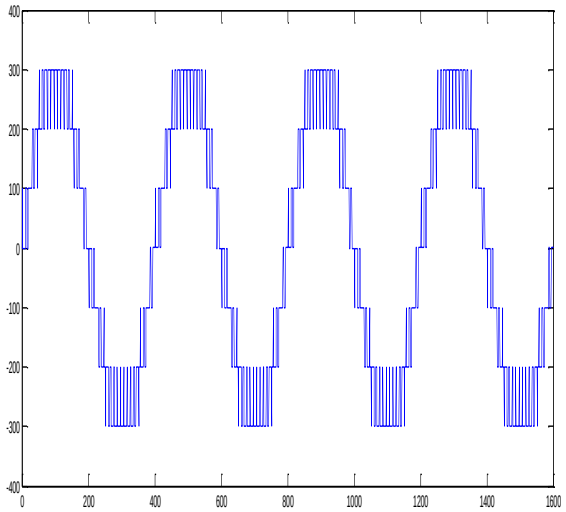

Fig.7 Output waveform of seven level Inverter

RMS VALUE OF OUTPUT VOLTAGE = 213.5

FFT analysis of the Output voltage

The fundamental frequency (50 Hz) = 296.5 and THD = 19.27%

FFT of output voltage of seven level Inverter

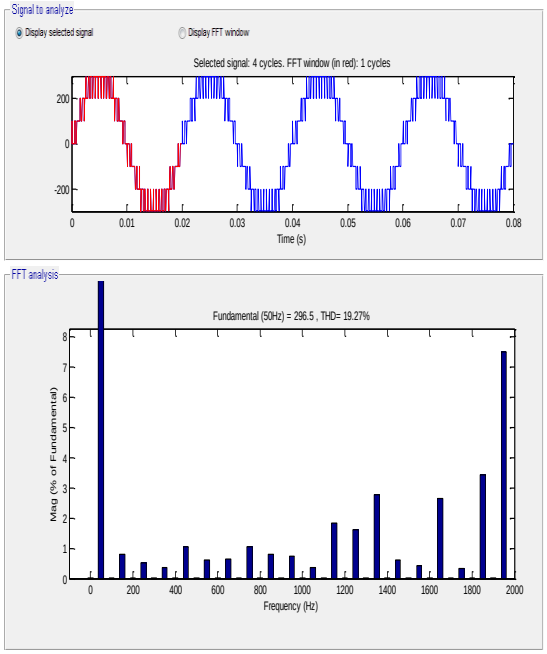

Fig.8 FFT of output voltage of seven level Inverter

VI. Conclusions

A new inverter topology has been proposed which has superior features over conventional multilevel inverter topologies in terms of the required power switches and isolated dc supplies, control requirements, cost, and reliability. It is shown that this topology can be a good candidate for converters used in high power applications such as FACTS, HVDC, PV systems, UPS, etc. In conventional PD SPWM technique, with diode clamped 7-level inverter, 6 carrier signals are required. While in proposed topology, only three carriers are required. The presented results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM generation. This will add up to the efficiency of the converter as well as reducing the size and cost of the inverter. The Phase Disposition (PD) SPWM control method is used to drive the inverter. The PWM for this topology has fewer complexities since it only generates positive carriers for PWM control. The simulation results of the proposed seven-level inverters are presented in this paper.

References

[1] S. M. Metev and V.] K. Jang-Hwan, S.-K. Sul, and P. N. Enjeti

[2] "A carrier-based PWM method with optimal switching sequence for a multilevel four-leg voltage- source inverter," *IEEE Trans. Ind. Appl.*, vol.44, no. 4, pp. 1239–1248, Jul./Aug. 2008.

[3] S. Srikanthan and M. K. Mishra, "DC capacitor voltage equalizationin neutral clamped inverters for DSTATCOM application," *IEEE Trans.Ind. Electron.* vol. 57,

[4] K. Nakata, K. Nakamura, S. Ito, and K. Jinbo, "A three-level traction inverter with IGBTs for EMU," in *Conf. Rec. IEEE IAS Annu.Meeting*, 1994, vol. 1, pp. 667–672.

[5] E. Najafi and A. H. M. Yatim, "A novel current mode controller for astatic compensator utilizing Goertzel algorithm to mitigate voltage sags,"*Energy Convers. Manage.*, vol. 52, no. 4, pp. 1999–2008, Apr. 2011.

[6] S. G. Song, F. S. Kang, and S.-J. Park, "Cascaded multilevel inverterEmploying three-phase transformers and single dc input," *IEEE Trans.Ind. Electron.* vol. 56, no. 6, pp. 2005–2014, Jun. 2009.

[7] P. Barbosa, P. Steimer, J. Steinke, L. Meysenc, M. Winkelnkemper, And N. Celanovic, "Active neutral-point-clampe multilevel converters," in *Proc. IEEE 36th Power Electron Spec. Conf.*, 2005, pp. 2296–2301.

[8] A . Radan, A. H. Shahirinia, and M. Falahi, "Evaluation of carrier- Based PWM methods for multi-level inverters," in *Proc. IEEE ISIE*, 2007,pp. 389–394.

[9] R. Stala, "Application of balancing circuit for dc-link voltages balance ina single-phase diode-clamped inverter with two three-level legs," *IEEETrans. Ind. Electron.*, vol. 58, no. 9, pp. 4185–4195, Sep. 2011.

[10] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photo- voltaic systems with fuzzy logic control," *IEEE Trans. Ind. Electron.*, vol. 57, no. 12, pp. 4115–4125, Dec. 2010.

[11] C. Govindaraju and K. Baskaran, "Analysis and implementation of multiphase multilevel hybrid single carrier sinusoidal modulation," *J. Power Electron.*, vol. 10, no. 4, pp. 365–373, Jul. 2010.

[12] C. Cecati, F. Ciancetta, and P. Siano, "A multilevel inverter for photo- voltaic systems with fuzzy logic control," *IEEE Trans. Ind. Electron.*, . 57, no. 12, pp. 4115-4125, Dec. 2010.

[13] G.-J. Su, "Multilevel dc-link inverter," *IEEE Trans. Ind. Appl*., vol. 41 no. 3, pp. 848–854, May/Jun. 2005.

[14] J.-S. Lai and F. Z. Peng, "Multilevel converters-a new breed of power converters," *IEEE Trans. Ind. Appl.*, vol. 32, no. 3, pp. 509–517, May/Jun. 1996.

[15] C.A.C. Cavaliere , E. H. Watanabe, and M. Aredes, "Multi-pulse STATCOM operation under unbalanced voltages," in *Proc. IEEE Power Eng. Soc. Winter Meeting*, 2002, vol.1, pp. 567–572.

[16] P. Veiko, *Laser Assisted Microtechnology*, 2nd ed., R. M. Osgood, Jr., Ed. Berlin, Germany: Springer-Verlag, 1998.

Author's profile

Shadma Khan*, received B.E. from TRUBA Institute of Engg. & Information technology (T.I.E.I.T), affiliated to RGTU, Bhopal and currently pursuing M.Tech. In POWER SYSTEM from OIST, affiliated to RGTU, Bhopal. Her area of interests is Power System, Electrical Machines.*

Monika Jain *received M.Tech. Degree with Specialization in POWER SYSTEM.. She has worked as a Assistance Professor in oriental institute of science and technology, affiliated to R.G.P.V University.*