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Design of CMOS Broadband Transimpedance Amplifier with Regulated Cascode and Series Inductive Peaking

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Abstract *– This paper presents a new topology of Transimpedance amplifier using regulated cascode (RGC) stage with series inductive peaking for the enhancement of overall bandwidth of TIA and lowering the level of input referred noise current spectral density. TIA is able to achieve low input impedance because of RGC stage. TIA also employs series inductive peaking techniques for bandwidth enhancement by lowering the effect of junction capacitance of photodiode. Simulated transimpedance gain is 67.2 dbΩ with -3db bandwidth of about 9.5 GHz. The simulated input referred noise current spectral density is 10 pA/√Hz.*

Keywords*: Broadband, regulated cascade (RGC), bandwidth extension, transimpedance amplifier (TIA)*

I. Introduction

Fiber optic communication has migrated from telephony and wide-area-network infrastructure where low attenuation allows long distances and large bandwidth of silica fibers maintains high information capacity to shorter scales such as storage area networks, memory links, and even for chip-scale global signals where processing requirements demand bandwidth not achievable over electrical interconnects [1]. THE dramatic growth of data transportation volume and speed over the internet in recent years entails the development of low cost integrated optical communication systems with ever-increasing transmission bandwidth. Currently, the most successful high-speed digital communication protocol is SONET OC-192 while the 10-Gb/s Ethernet (IEEE 802.3ae) is also emerging as an alternative for point-to-point applications [2].

The CMOS implementation of optical transceivers is particularly attractive because they can be integrated in the same chip as the digital processing units, resulting in lower cost and power consumption. Transimpedance amplifier (TIA) is the first gain stage and one of the essential blocks in an optical receiver. The design of a wideband TIA is challenging mainly because it is driven by a photodetector with high capacitance, usually ranging from 0.2 to 0.5 pF [15]. The TIA converts current from a photodetector to generate an output voltage. Since a single TIA stage is typically insufficient to amplify the input current to logical voltage levels, the MA provides additional voltage gain to amplify the signal to the desired signal swing [4]. Among all the challenges in the design of fully integrated CMOS broad-band TIAs, sufficient bandwidth with small gain ripple is of first priority and low-noise is second because the noise of the preamplifier dominates that of the whole receiver. Due to the inferior parasitic and noise characteristics of CMOS technology, many circuit techniques have been studied in CMOS TIA design to achieve comparable performances to those III/V or SiGe counterparts [2]. In this paper, we introduce a new technique to boost the TIA bandwidth by using RGC stage followed by series inductive peaking and capacitive degeneration technique.

In Section II, the Broadband design techniques and the design of proposed TIA is discussed, in Section III, the simulation results of the proposed structure is presented and discussed. Finally, in Section IV, conclusion is provided with possible future improvement.

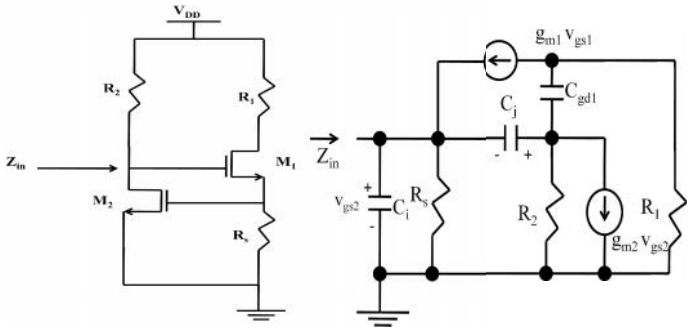
II. Broad-band Design Techniques of TIA

II.1. RGC Stage

The RGC input stage in fig. 1(a) is well suited for broad-band TIA design by its very low input impedance, which could be derived from small signal circuit model in fig. 1(b).

where, $C_i \approx C_{sb1} + C_{gs2}$ and $C_j \approx C_{gs1} + C_{gd2}$. The small signal input resistance is therefore given by

$$r_i = Z_{in}(0) \approx \frac{1}{g_m(1 + g_{m2} R_2)} \quad (1)$$



(a) (b)

Fig. 1 RGC stage. (a) Circuit schematic. (b) Small- Signal model

This very small input impedance in large part isolates the photodiode capacitance from bandwidth determination and therefore, unlike common gate or common source TIAs, the dominant pole of an RGC TIA is usually located within the amplifier rather than at the input node[9].

II.2. Capacitive Degeneration Stage

The capacitive degeneration network formed by R_S and C_S introduces an additional peaking in the frequency response. Considering it as a simple common source amplifier, the location of the zero is obtained as

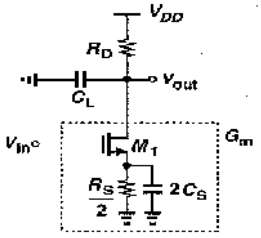


Fig. 2. Capacitive Degeneration Stage

The voltage gain of a gain stage with capacitive degeneration is expressed by

$$A_v = \frac{V_{out}}{V_{in}} = \frac{g_{m1} R_1}{1 + g_{m1} R_s} \frac{1 + sR_sC_s}{1 + s\frac{R_sC_s}{1 + g_{m1}R_s}} \quad (2)$$

which contributes a zero at $\frac{1}{R_sC_s}$ and a pole at

$(1+ g_{m1}R_s) /R_s C_s$. The zero could be used to compensate the dominant pole of the circuit. The -3 dB cutoff frequency is therefore determined by the second lowest pole of the circuit.

II.3 Series Inductive Peaking

Series peaking L1 inductor are adopted for the proposed TIA to increase the BWER by reducing the capacitive loading effect of the photodiode [8].

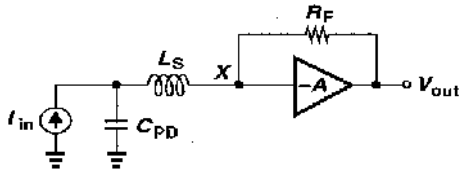


Fig. 3. Series Inductive Peaking

$$\frac{V_{out}}{V_{in}} = \frac{-1}{S^2 + \frac{R_F}{(A+1)L_S}S + \frac{1}{C_{PD}L_s}} \frac{AR_F}{(A+1)C_{PD}L_S} \quad (3)$$

$$\omega_{-3dB} \approx \frac{\sqrt{2}\,A}{R_F C_{PD}} \quad (4)$$

II.4 Noise Analysis

The equivalent input noise current, also called input-referred noise current, is a significant figure of merit of TIAs in that it directly affects the optical link budget. The bit error rate (BER) of an optical front-end can be expressed in terms of the total equivalent input noise current $i_{total,n,eq}$ by

$$BER = Q\left(\frac{i_{in,pp}}{2i_{total,n,eq}}\right) \quad (5)$$

where, $i_{in,pp}$, is the peak to peak input current signal amplitude and $Q(x) = \int_x^\infty (\frac{1}{\sqrt{2\pi}}) \exp(-(x^2/2))\, dx$. The equivalent input noise current is defined in such a way that together with a noiseless TIA, it reproduces the same output noise as the actually noisy TIA. Although the TIA noise model can be conveniently represented by a noise current source only, the equivalent input noise current is dependent on the source impedance, which is mainly determined by the photodiode capacitance and the matching network [6].

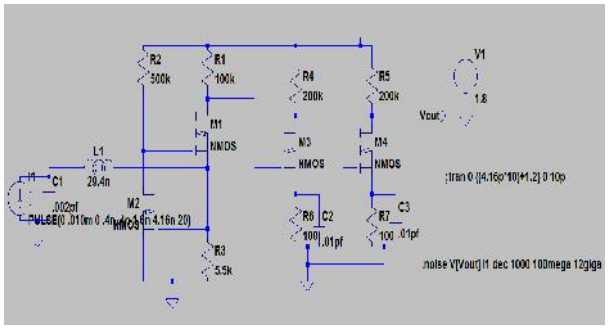


Fig. 4. Circuit of Proposed Transimpedance Amplifier

III. Simulation Results of Proposed TIA

The three broad- band design techniques introduced in section II are combined together to design a high performance TIA in this section. RGC input stage consist of two NMOS transistor M1 and M2 provide low input impedance in TIA.
Inductive series peaking in the circuit employed by using inductor L1 provides peaking effect and enhances the bandwidth [12]. Two stages of capacitive degeneration employed by using NMOS M3 and M4 enhances the overall bandwidth and TIA is capable to operate in high frequency ranges. Also this design is capable to reduce the equivalent input noise current below a certain limit [14].

The input current of a photo diode is small, in the order of micro-amperes, which necessitates low input impedance for the RGC block. RGC circuit is a common gate amplifier with a local feedback [5]. The local feedback formed by M1 and R3 for the upper RGC circuit is a common source amplifier, which generates a negative feedback voltage at the gate of M2. The feedback increases the effective transconductance (gm) of the common gate amplifier to reduce the input resistance [10]. Reduction of the input resistance also isolates the input pole associated with the large parasitic capacitance Cpd. It reduces the impact on the TIA bandwidth to result in an improved frequency response.

The second stage of the proposed TIA consists of a capacitive degenerate M3 and M4. The stage intends for bandwidth compensation in order to increase the gain-bandwidth product. The capacitive degeneration introduces a high-frequency peaking zero to the system, and the feedback network further increases the bandwidth by a factor of (1 + loop-gain) [11].

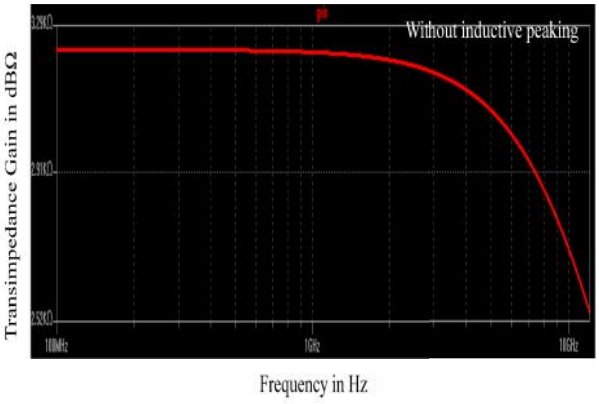


Fig. 4 Simulation of transimpedance gain without series inductor

In fig.4. Simulation of proposed TIA can be showed without using series inductor which results less gain and bandwidth.

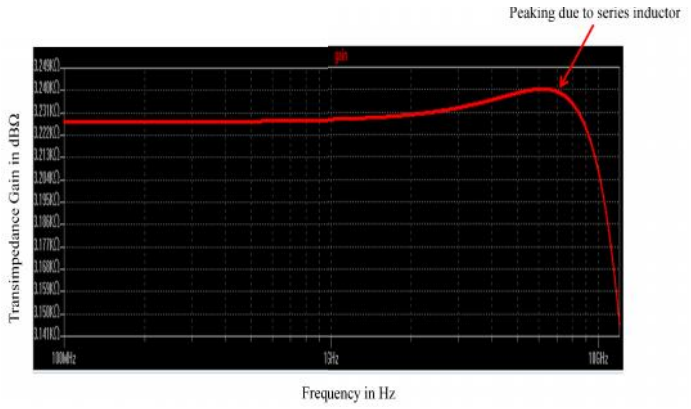


Fig. 5. Simulation of transimpedance gain with series inductor

In fig.5 simulation of transimpedance gain is observed by employed series inductor. -3db gain of TIA with series inductor is 67.2 dBΩ at frequency 9 GHz. So by apply series inductor bandwidth of TIA can be increased.

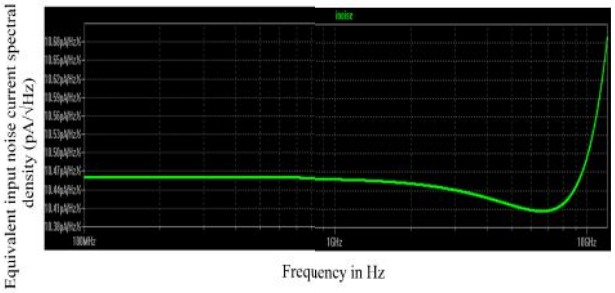


Fig. 6. Simulation of Equivalent input noise current spectral density

In fig. 6 shows the simulation of input noise current spectral density it can be observed 10.44 pA√Hz.

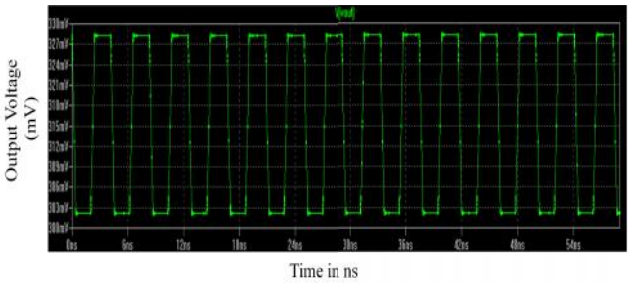


Fig. 7. Simulation of output voltage

In Fig.7 Simulation result shows the amplified output voltage observed 328.34mV in response to 10µA input current.

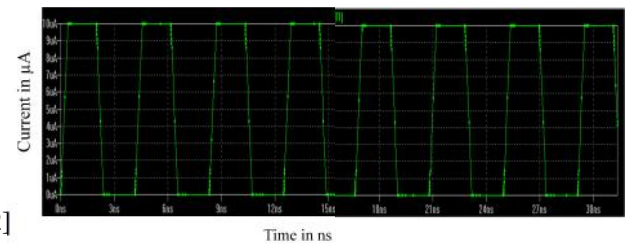


Fig. 8. Simulation of input current

Fig. 8 shows the simulation of input current which is equivalent to photodiode output current.

Performance comparison of TIAs

Design	**Bandwidth (GHz)**	**Gain dBΩ**	**Input-Referred noise pA/√Hz**	**Power Dissipation (mw)**
[6]	8	63.3	6.5	500
[8]	9	55	14	140
[7]	9.2	54	17	130
[2]	8	53	18	13.5
This Design	9.5	67.2	10	37.7(μw)

IV. Conclusion

A bandwidth enhancement method for broad-band TIA design is proposed, which is based on a unique combination of series inductive, capacitive degeneration, RGC input stage. Simulation results of transimpedance gain is 67.2 dBΩ. The simulated value of input referred noise current is 10 pA/√Hz. Overall bandwidth is found to be 9.5 GHz. Amplified output voltage is 328.34mV. In future bandwidth and data rate of TIA will be enhanced by using cascade stages of RGC and capacitive degeneration with series and shunt inductive peaking techniques.

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