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Design of CMOS Broadband Transimpedance Amplifier with Cross Coupled Current Conveyor and series inductive Peaking

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Abstract *– This paper hearsay a unique cross-coupled current conveyor based cmos transimpedance amplifier with series inductive peaking design to achieve an input capacitive load insensitive, low noise and augment the bandwidth of transimpedance amplifier. The peaking inductor is in series with the capacitor constituting a dominant pole. It boosts the band width of the amplifier.The whole transimpedance amplifier consumes 225.90µW of the dc power measured results show a -3dB bandwidth of about 6.7GHz with a 0.25pF photodiode capacitance. The trnsimpedance gain for positive output port is 50.9 dBΩ . The measured single ended input referred noise current spectral density is kept underneath 4.4159pA/√Hz within the TIA frequency band. The series inductive peaking network consists of inductor at the input to resonate with C_D near the -3dB bandwidth of the amplifier, reduces input referred noise and increase the overall bandwidth.*

Keywords*: Transimpedance amplifier, noise, gain, bandwidth enhancement, cross coupled current conveyor, series inductive peaking.*

I. Introduction

Fiber optic communication has migrated from telephony and wide-area-network infrastructure where low attenuation allows long distances and large bandwidth of silica fibers maintains high information capacity to shorter scales such as storage area networks, memory links, and even for chip-scale global signals where processing requirements demand bandwidth not achievable over electrical interconnects [1].The dramatic growth of data transportation volume and speed over the Internet in recent years entails the development of low cost integrated optical communication systems with ever-increasing transmission bandwidth [2].Therefore, optical communication systems operating at 10 Gb/s are of great interest. Transimpedance amplifiers (TIAs) are extensively exploited as the front-end of optical communication receivers. Traditionally, such front-end circuits and devices are heavily dependent on III/V technologies due to their speed and noise advantages. However, the demand for high volume and wide deployment of optical components in recent years makes silicon based integrated circuits the most economical solution [2].

CMOS process technology gives low power, low cost and high yield which offers the most

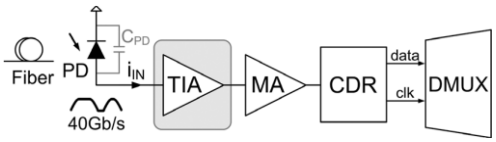

Fig. 1. Block diagram of an optical receiver.

economical solution in the consumer application market [3].The design of wide band TIA is the challenging mainly because it is driven by a photo detector with high capacitance usually ranging from 0.2 to 0.5 pF [4].The specification requirements of a typical TIA are large bandwidth, high transimpedance gain, low noise, low power consumption, and small group delay variation [5]. Among these designing parameters, large bandwidth is critical to achieve broadband data transmission link. Hence, methods for bandwidth enhancement are reported constantly [3]. The major bandwidth restriction of a

conventional TIA is usually at the input node due to the large capacitive load introduced by preceding photodiode. To capture sufficient optical power, large area photodiode is evitable, bringing large junction capacitance. Various CMOS TIA architectures have been reported that essentially explore different input stages for isolating the large input capacitance of the photodiode from bandwidth determination, such as common gate (CG) input stage [6], regular cascade (RGC) stage [6], [7], or CG feed forward topology containing negative feedback [6]. Other bandwidth enhancement techniques, such as inductive peaking [3] and capacitive degeneration [7], are also implemented. However, the bandwidth of all reported TIAs reduces with increasing photodiode's capacitance. This paper describes a novel bandwidth enhancement method by using series inductive peaking at the input stage and low input referred noise by cross coupled current conveyor stage in design.

In Section II, the detailed circuit design and analysis of the proposed TIA is discussed; in Section III, the simulation and measurement results of the proposed structure is presented and discussed. Finally, in Section IV, conclusion is provided with possible future improvement.

II. Design and analysis of Proposed TIA

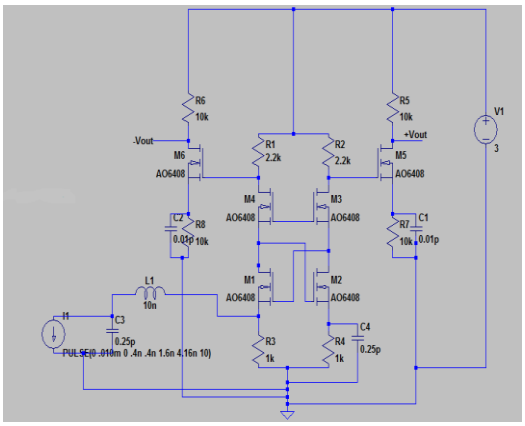

Fig. 2. Schematic of Proposed TIA.

II.1. Series Inductive Peaking

Series inductive peaking is another technique for extending TIA band width. An inductor can be interposed between a photodiode and the input of a transimpedance amplifier so as to increase the bandwidth [8].

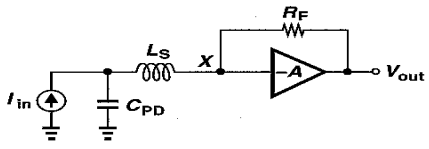

Fig. 3. Series inductive peaking

$$\left[\frac{-V_{out}}{A} - \left(V_{out} + \frac{V_{out}}{A}\right)\frac{L_S S}{R_F}\right] C_{PD} S$$

$$= I_{in} + \left(V_{out} + \frac{V_{out}}{A}\right)\frac{1}{R_F}$$

$$\frac{V_{out}}{I_{in}} = \frac{-1}{S^2 + \frac{R_F}{(A+1)L_S}S + \frac{1}{C_{PD}\,L_S}} \frac{AR_F}{(A+1)C_{PD}\,L_S}$$

$$\omega_{-3db} \approx \frac{\sqrt{2}\,A}{R_F\,C_{PD}}$$

Thereby increasing the bandwidth by approximately 41% with and overshoot of 4.3% [9].

II.2. Cross Coupled Current Conveyor Stage

A new technique to offset the large junction capacitance brought by photodiode. It is achieved by "creating""zero differential impedance" at the input node of a TIA. This input stage is based on a cross-coupled current conveyor structure [10]. It provides a stable performance over a wide range capacitive load. Cross coupled structure also brings a huge improvement in noise performance [3].

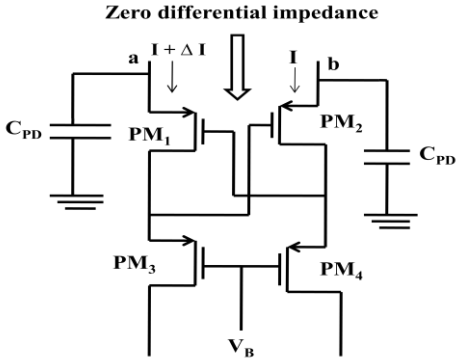

Fig. 4. Current Conveyor Stage

When the four PMOS PM1, PM2, PM3, and PM4 are in saturation region, ideally

$$V_{sg}\,1 = V_{sg}\,3 = V1 \text{ and } V_{sg}\,2 = V_{sg}\,4 = V2$$

Suppose the bias voltage VB is 0-V first, the voltage at node a, Va and the voltage at node b, Vb are

$$\text{Va} = V_{sg}\,1 + V_{sg}\,4 = \text{V1} + \text{V2}$$
$$\text{Vb} = V_{sg}\,2 + V_{sg}\,3 = \text{V2} + \text{V1}$$

Thus

$$\text{Va} = \text{Vb}$$

Thus, no matter how large the current difference between node a and b is, ΔZ will be zero, which is independent of Δi and the parasitic capacitance of the four transistors. If the same capacitors with capacitance C_{PD} are added to nodes a, b, respectively, ΔZ will still be zero since Va = Vb. This unique property of cross-coupled PMOS current conveyor is referred as "zero differential impedance."[3]

II.3. Capacitive Degeneration

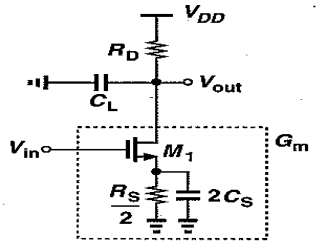

Fig. 5. Capacitive Degeneration Stage

Besides pushing the dominant pole to higher frequencies to increase the bandwidth, it is also possible to compensate the dominant pole with a zero, which could be accomplished by capacitive degeneration. The zero could be used to compensate the dominant pole of the circuit. The 3-dB cutoff frequency is therefore determined by the second lowest pole of the circuit [3]. The zero introduced by the capacitive degeneration stage is then to satisfy the following equation:

$$z = \frac{1}{2\pi R_S C_S} = \mathrm{f}$$

Besides the zero, this capacitive degeneration stage also brings an additional pole at:

$$\mathrm{f_s} = \frac{1 + \mathrm{g_m R_S}}{2\pi R_S C_s}$$

III. Simulation Results and Discussions

III.1.Gain and Input noise of Proposed TIA

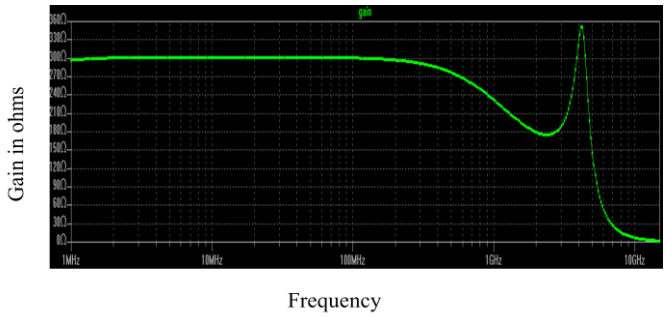

Fig. 6. Simulation result of Gain and bandwidth

At the input stage of the proposed TIA design utilizes the bond wire inductance on-chip spiral inductance can be used to realize this inductor. L_1 to create inductive peaking at the input chosen to resonate with C_3 which can be treated as photodiode junction capacitance near -3dB bandwidth of the amplifier, L_1 both reduces the input referred noise and increases the overall band width. -3 dB bandwidth of proposed transimpedance amplifier is.7 GHz and input referred noise reduces to *4.4159 pA/√Hz.*

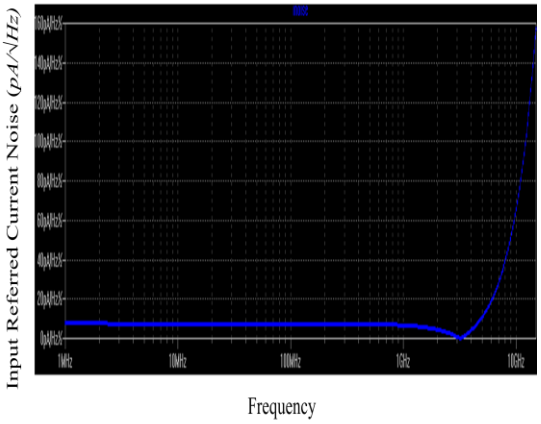

Fig. 7. Simulation result of Input referred current noise

The noise characteristics of the transimpedance preamplifier in terms of the input referred noise current spectral density or the equivalent input noise current spectral density is of primary importance in the determination of the sensitivity of the whole optical receiver front-end [9], [10]. It is well-known that besides bandwidth extension, the input series inductor can also help to reduce the equivalent input noise [11], [12], [13]. The total equivalent input noise current spectral density of the propose TIA input stage with series inductive peaking can be obtained by summing up the respective noise components.

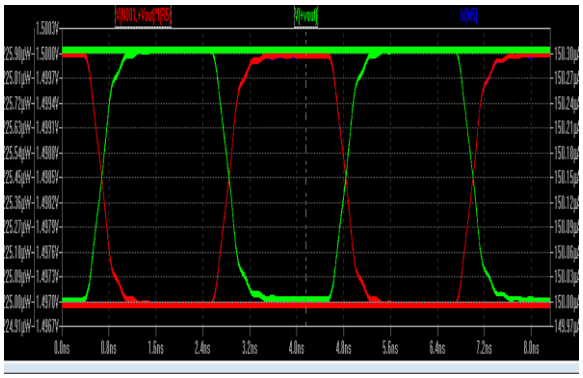

Fig. 8. Measured Eye Diagram.

Fig. 8 shows the eye diagram of the positive output terminal 4.65 Gb/s. The output has a peak-to peak value around 1.49 V with input level to be 150 μA, and it has a peak-to-peak jitter of 28 ps. A bit-error-rate of 10−12, which is corresponds to an optical sensitivity of −15 dBm, assuming the optical responsivity of photodiode to be 0.3 A/W.

TABLE I
PERFORMANCE COMPARISON OF CMOS TIAS

References	C_{PD} (pf)	Gain (dBΩ)	Power consu-mption (mW)	BW (GHz)	Input-referred noise (pA/√Hz)
[14]	0.15	53.9	19.6	7.7	5.8
[7]	0.25	61	70.2	7.2	8.2
[3]	0.25	46	10.7	4	10
This Work	0.25	50.9	0.225	6.7	4.4

IV. Conclusion

The proposed TIA design offers new technology by combining both series inductive peaking and cross coupled current conveyor for the improvement in input noise and band width, further the bandwidth of the TIA can be increased by using capacitive degeneration stage. The noise analysis also shows that the proposed input stage achieves more effective isolation of the photodiode capacitance from the bandwidth determination as compared to CG and RGC input stages. The cross-coupled structure facilitates the construction of a differential TIA circuit as well. Further the improvement can be done by using cross coupled current conveyor II stage (CCII) in input referred noise of the TIA. For the fabrication of circuit use bond wire inductance occupies less area on the chip and better the speed of the device.

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