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Review Work on Vedic Multiplier Based 16×16 Multiplier

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Abstract *– The need of low area and high speed Multiplier is increasing as the need of high speed processors are needed. Vedic arithmetic is that the traditional system of arithmetic which has a novel technique of calculations supported sixteen Sutras that are discovered by Sri Bharti Krishna Tirthaji. Any processor's performance depends on 3 vital factors specifically speed, space and power. a higher trade-off between these factors makes the processor, a good one. Multipliers are the usually used architectures within the processor. If the performance of those multipliers is improved then powerful processors is created in future. During this work, the planned number style supported the sutra- 'Urdhva Tiryakbhyam' of Vedic arithmetic is analyzed and also the performance results of the number are compared with standard multipliers. The multipliers used in Square and cube architecture have to be more efficient in area and also in speed. In this proposed work a multiplier is implemented based on Nikhilam sutra with binary excess unit. The ripple carry adder in the multiplier architecture increases the speed of addition of partial products. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2. The proposed architecture of this paper analysis the logic size, area and power consumption using Xilinx 14.2.*

Keywords*: Vedic Mathematics ,Vedic Multiplier, Array Multiplier, MAC, Nikhilam Sutra*

I. Introduction

Arithmetic is the oldest and most elementary branch of Mathematics. The name Arithmetic comes from the Greek word άριθμός (arithmos). Arithmetic is used by almost everyone, for tasks ranging from simple day to day work like counting to advanced science and business calculations. As a result, the need for a faster and efficient Arithmetic Unit in computers has been a topic of interest over decades. The work presented in this thesis, makes use of Vedic Mathematics and goes step by step, by first designing a Vedic Multiplier, then a Multiply Accumulate Unit and then finally an Arithmetic module which uses this multiplier and MAC unit. Multiplication basically is the mathematical operation of scaling one number by another. Talking about today's engineering world, multiplication based operations are some of the frequently used Functions, currently implemented in many Digital Signal Processing (DSP) applications such as Convolution, Fast Fourier Transform, filtering and in Arithmetic Logic Unit (ALU) of Microprocessors. Since multiplication is such a frequently used operation, it's necessary for a multiplier to be fast and power efficient and so, development of a fast and low power multiplier has been a subject of interest over decades. The multiplier factor design relies on the Vertical and Crosswise algorithmic rule of antique Indian Vedic arithmetic. Several Digital signal processing (DSP) systems includes multipliers jointly of core hardware blocks. Multipliers hold a major role in numerous DSP applications like digital filtering; electronic communication and fast Fourier transform [4]. The common classification of multipliers betting on their design involves 3 types: 'serial multipliers', 'parallel multipliers' and 'serial-parallel multipliers'. During this work, multiplier factor design supported Urdhva tiryakbhyam Sanskrit literature [6],a concept supported Vedic arithmetic is mentioned. Multiply Accumulate or MAC operation is also a commonly used operation in various Digital Signal Processing Applications. Now, not only Digital Signal Processors, but also general-purpose Microprocessors come with a dedicated Multiply Accumulate Unit or MAC unit. When talking about the MAC unit, the role of Multiplier is very significant because it lies in the data path of the MAC unit and its

operation must be fast and efficient. A MAC unit consists of a multiplier implemented in combinational logic, along with a fast adder and accumulator register, which stores the result on clock.

II. Vedic Mathematics

Vedic mathematics is part of four Vedas (books of wisdom). It is part of Sthapatya- Veda (book on civil engineering and architecture), which is an upa-veda (supplement) of Atharva Veda. It gives explanation of several mathematical terms including arithmetic, geometry (plane, co-ordinate), trigonometry, quadratic equations, factorization and even calculus.

His Holiness Jagadguru Shankaracharya Bharati Krishna Teerthaji Maharaja (1884- 1960) comprised all this work together and gave its mathematical explanation while discussing it for various applications. Swamiji constructed 16 sutras (formulae) and 16 Upa sutras (sub formulae) after extensive research in Atharva Veda. Obviously these formulae are not to be found in present text of Atharva Veda because these formulae were constructed by Swamiji himself. Vedic mathematics is not only a mathematical wonder but also it is logical. That's why it has such a degree of eminence which cannot be disapproved. Due these phenomenal characteristics, Vedic maths has already crossed the boundaries of India and has become an interesting topic of research abroad. Vedic maths deals with several basic as well as complex mathematical operations. Especially, methods of basic arithmetic are extremely simple and powerful [2, 3].

The word "Vedic" is derived from the word "Veda" which means the store-house of all knowledge. Vedic mathematics is mainly based on 16 Sutras (or aphorisms) dealing with various branches of mathematics like arithmetic, algebra, geometry etc[15]. These Sutras along with their brief meanings are enlisted below alphabetically.

1. (Anurupye) Shunyamanyat – If one is in ratio, the other is zero.
2. Chalana-Kalanabyham – Differences and Similarities.
3. Ekadhikina Purvena – By one more than the previous One.
4. Ekanyunena Purvena – By one less than the previous one.
5. Gunakasamuchyah – The factors of the sum is equal to the sum of the factors.
6. Gunitasamuchyah – The product of the sum is equal to the sum of the product.
7. Nikhilam Navatashcaramam Dashatah – All from 9 and last from 10.
8. Paraavartya Yojayet – Transpose and adjust.
9. Puranapuranabyham – By the completion or noncompletion.
10. Sankalana- vyavakalanabhyam – By addition and by subtraction.
11. Shesanyankena Charamena – The remainders by the last digit.
12. Shunyam Saamyasamuccaye – When the sum is the same that sum is zero.
13. Sopaantyadvayamantyam – The ultimate and twice the penultimate.
14. Urdhva-tiryagbhyam – Vertically and crosswise.
15. Vyashtisamanstih – Part and Whole.
16. Yaavadunam – Whatever the extent of its deficiency

III. Vedic Multiplication

General 2X2 Vedic Multiplier[3] : The method is explained below for two, 2 bit numbers A and B where A = a1a0 and B = b1b0 as shown in Figure 2. Firstly, the Least Significant Bits are multiplied which gives the Least Significant Bit (LSB) of the final product (vertical). Then, the LSB of the multiplicand is multiplied with the next higher bit of the multiplier and added with, the product of LSB of multiplier and next higher bit of the multiplicand (crosswise). The sum gives second bit of the final product and the carry is added with the partial product obtained by multiplying the most significant bits to give the sum and carry. The sum is the thir corresponding bit and carry becomes the fourth bit of the final product.

$$s0 = a0b0 \quad (1)$$

$$c1s1 = a1b0 + a0b1 \quad (2)$$
$$c2s2 = c1 + a1b1; \quad (3)$$

The final result will be c2s2s1s0. This multiplication method is applicable for all the cases. The 2x2 bit Vedic multiplier (VM) module is implemented using four input AND gates & two half-adders which is displayed in its block diagram in Figure (1)

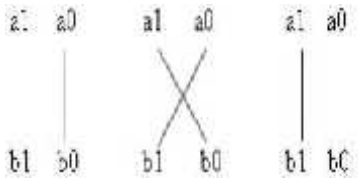

Figure 1: The Vedic Multiplication Method for two 2-bit binary numbers

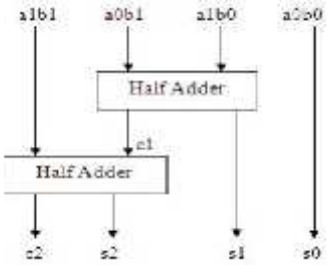

Figure 2: Block Diagram of 2x2 bit Vedic Multiplier (VM

IV. Array Multiplier

Array multiplier is an efficient layout of a combinational multiplier. In array multiplier, consider two binary numbers A and B, of m and n bits. There are mn summands that are produced in parallel by a set of mn AND gates. n x n multiplier requires n (n-2) full adders, n half-adders and n2 AND gates. Also, in array multiplier worst case delay would be (2n+1) td. Array Multiplier gives more power consumption as well as optimum number of components required, but delay for this multiplier is larger. It also requires larger number of gates because of which area is also increased; due to this array multiplier is less economical .Thus, it is a fast multiplier but hardware complexity is high[2]

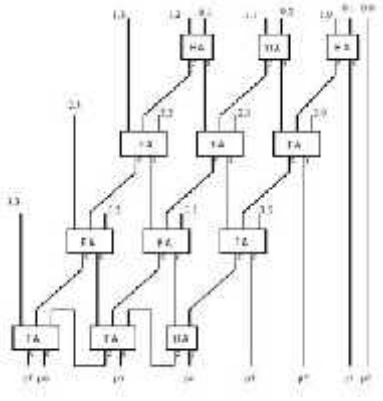

Figure 3 : Array Multiplier

V. Multiply Accumulate Unit (MAC)

Multiply-accumulate operation is one of the basic arithmetic operations extensively used in modern digital signal processing (DSP). Most arithmetic, such as digital filtering, convolution and fast Fourier transform (FFT), requires high-performance multiply accumulate operations. The multiply-accumulator (MAC) unit always lies in the critical path that determines the speed of the overall hardware systems. Therefore, a high-speed MAC that is capable of supporting multiple precisions and parallel operations is highly desirable.

1.1 Basic MAC architecture

Basically a MAC unit employs a fast multiplier fitted in the data path and the multiplied output of multiplier is fed into a fast adder which is set to zero initially. The result of addition is stored in an accumulator register. The MAC unit should be able to produce output in one clock cycle and the new result of addition is added to the previous one and stored in the accumulator register. Fig 1.1, below shows basic MAC architecture. Here the multiplier that has been used is a Vedic Multiplier built using Urdhva Tiryakbhyam Sutra and has been fitted into the MAC design.

1.2 Arithmetic Module

Arithmetic Logic Unit can be considered to be the heart of a CPU, as it handles all the mathematical and logical calculations that are needed to be carried out.

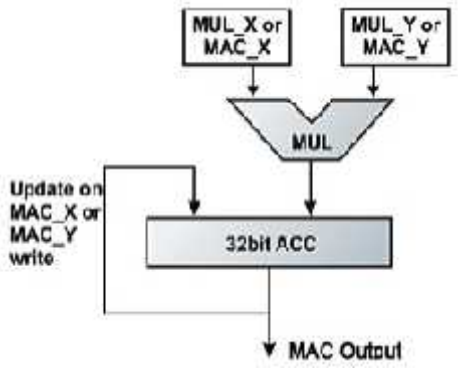

Fig 4. Basic MAC unit

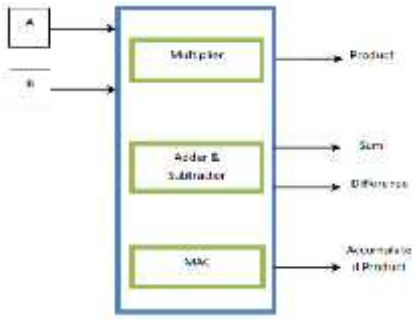

Fig 5 Basic block diagram of Arithmetic unit

Again there may be different modules for handling Arithmetic and Logic functions. In this work, an arithmetic unit has been made using Vedic Mathematics algorithms and performs Multiplication, MAC operation as well as addition and subtraction. For performing addition and subtraction, conventional adder and subtractor have been used. The control signals which tell the arithmetic module, when to perform which operations are provided by the control unit, which is out of the scope of this thesis. It is shown in fig.1.2

1.6 Early Indian Mathematics

The early Indian mathematicians of the Indus Valley Civilization used a variety of intuitive tricks to perform multiplication. Most calculations were performed on small slate hand tablets, u sing chalk tables. One technique was of lattice multiplication. Here a table was drawn up with the rows and columns labeled by the multiplicands. Each box of the table is divided diagonally into two, as a triangular lattice. The entries of the table held the partial products, written as decimal numbers. The product could then be formed by summing down the diagonals of the lattice. This is shown in Fig 1.3 below

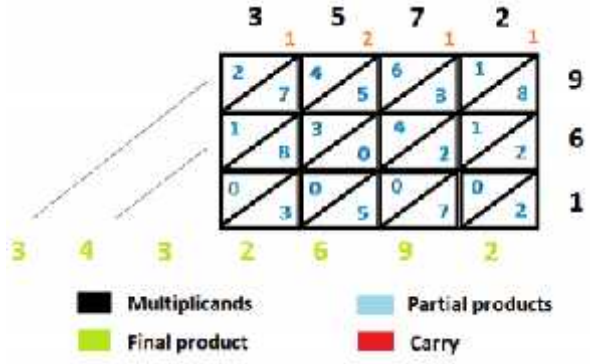

Fig.6 Example of Early Multiplication Technique

II.Literature Survey

S.P.Pohokar et. al[1] "Design and Implementation of 16 x 16 Multiplier Using Vedic Mathematics" in this paper Vedic Multiplier is efficient than Array Multiplier. As the number of bit increases from 8 x 8 bit to 16 x 16 bit, the timing delay greatly reduces for Vedic multiplier as compared to array multiplier. The time delay in Vedic multiplier for 16 x 16 bit number is 28.779 ns while the time delay for Array multiplier is 61.241 ns respectively. The memory required for 16 x 16 bit Vedic multiplier is 169924 kilobytes and Array multiplier required 178492 kilobytes. Thus Vedic multiplier shows the improved speed among the conventional multiplier and it also reduces the memory of the system. In future, this work could be extended to design and implement of Digital filters like FIR, IIR and frequency domain transformations like FFT and DCT algorithms.

Sudeep et. al [2] "Design and FPGAImplementation of High Speed Vedic Multiplier", Multiplication is an operation abundant required in Digital Signal method for numerous applications. This paper puts forward a high speed Vedic multiplier that is economical in terms of speed, making use of Urdhva Tiryagbhyam, a Sanskrit literature from Vedic maths for multiplication and Kogge Stone algorithm for humanities addition of partial product and in addition compares it with the characteristics of existing many algorithms**.**

G.Vaithiyanathan, et. al. [3] "Simulation and Implementation of Vedic multiplier factor exploitation VHDL Code" during a typical processor, Multiplication is one in every of the essential arithmetic operations and it wants well a great deal of hardware resources and quantity than addition and subtraction. In detail, 8.72% of all the instruction in typical method units is multipliers. In computers, a typical central process unit devotes a substantial quantity of your time interval in implementing arithmetic operations, considerably multiplication operations.

G.Ganesh Kumar, et. al. [4] "Design of High Speed Vedic Multiplier using Vedic Mathematics Techniques" it provides the planning of high speed Vedic number exploitation the techniques of Ancient Indian Vedic arithmetic that are customised to induce higher performance. Vedic arithmetic is that the ancient system of arithmetic that includes a distinctive technique of calculations supported sixteen Sutras**.**

Manoranjan Pradhan et. al [5] "Speed Comparison of 16x16 Vedic Multipliers", in this paper provides the extends multiplication to 16×16 Vedic multiplier factor exploitation "Nikhilam Sutra" technique. The 16×16 Vedic multiplier factor half victimization Urdhva Tiryagbhyam Sanskrit literature uses four 8×8 Vedic multiplier factor modules; one 16 bit carry save adders, and two 17 bit full adder stages. The carry save adder within the multiplier factor design will increase the speed of addition of partial product.

Jagadguru Swami Sri Bharti Krishna Tirthaji Maharaja et. al. [6] "Vedic arithmetic or Sixteen easy Mathematicle Formulae from the Veda", the utilization of Vedic arithmetic lies within the undeniable fact that it reduces normal|the quality} calculation within the standard arithmetic to terribly simple once. This will be

so as a result of the Vedic formulae have claimed to be building on the natural principles on that the human mind works. Vedic arithmetic is also a many effective algorithms that has cowl to various branches of engineering like computing. during this work, I even have studied fully completely different multipliers, which offer low power demand and high speed, jointly offer information of "urdhva-Tiryabhyam" algorithmic rule of ancient Indian Vedic arithmetic, that has used for multiplication to reinforce speed, space parameters of multipliers.

Nageswararao Chintapanti et al.[7]"New BEC Design for Efficient Multiplier," In this paper the performance of different types of adders is analysed. And carry select adder (CSLA) is the lowest delay compare to other adders. Carry select adder is one of the fastest adders used in many data processing processors to perform fast arithmetic functions. From the structure of the CSLA, there is a possibility for increasing the speed and reducing the area and in the CSLA. This work uses a simple and efficient gate- level modification to significantly reduce the area and power of the CSLA. Based on this modification 8-, 16-, 32-, and 64-b CSLA architecture have been developed and compared with the regular CSLA architecture. The proposed design has increased speed and reduced area and power as compared with the regular CSLA with only a slight increase in the delay. This work evaluates the performance of the proposed designs in terms of delay, speed (frequency) and memory. The results analysis shows.

III. Method

Nikhilam Sutra factually means "all from 9 and last from 10". Although it is valid to all cases of multiplication, it is more capable when the numbers involved are big. Since it checks out the compliment of the large number from its adjacent base to perform the multiplication operation on it, better is the original number, lesser the complexity of the multiplication.

Nikhilam Sutra stipulates subtraction of a number from the nearest power of 10 i.e. 10, 100, 1000, etc. The power of 10 from which the difference is calculated is called the Base. These numbers are considered to be references to find out whether given number is less or more than the Base. If the given number is 104, the nearest power of 10 is 100 and is the base. Hence the difference between the base and the number is 4, which is Positive and it is called NIKHILAM.

Procedure for implementation multiplier using Nikhalam sutra: NIKALAM PROCEDURE for DECIMAL calculation: Follow the procedure as done in KCM and finally divide the LSB and MSB part keep the LSB part as it is and after carry save adder addition multiply with 100 to MSB value if is 2-digit number (or) multiply with 1000 if it is 3-digit value and so on.

Nikhilam Sutra literally means "all from 9 and last from 10". Although it is applicable to all cases of multiplication, it is more efficient when the numbers involved are large. Since it finds out the compliment of the large number from its nearest base to perform the multiplication operation on it, larger is the original number, lesser the complexity of the multiplication. We first illustrate this Sutra by considering the multiplication of two decimal numbers (96 * 93) in Fig 4.6. Where the chosen base is 100 which is nearest to and greater than both these two numbers.

The right hand side (RHS) of the product can be obtained by simply multiplying the numbers of the Column 2 (7*4 = 28). The left hand side (LHS) of the product can be found by cross subtracting the second number of Column 2 from the first number of Column 1 or vice versa, i.e., 96 - 7 = 89 or 93 - 4 = 89. The final result is obtained by concatenating RHS and LHS (Answer = 8928).

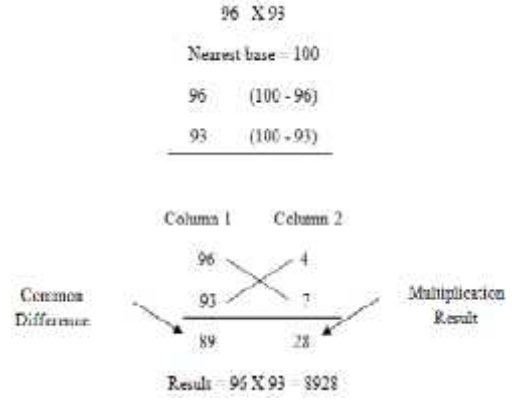

Fig.7 Multiplication Using Nikhilam Sutra

IV. Conclusion

Thus the proposed multiplier provides higher performance for higher order bit multiplication. This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results in terms of area and speed which improves the overall performance of the design. Nikhilam Sutra based Vedic multiplier with BEC is highly efficient algorithm for multiplication. This is mainly due to memory constraints. Effective memory implementation and deployment of memory compression algorithms can yield even better results. We have explored the possibility of applying the Nikhilam sutra of Vedic mathematics to binary number multiplication. We

can take advantage of the fact that this sutra can convert large-digit multiplication to corresponding small digit multiplication. Nikhilam method is particularly efficient when both multiplicand and multiplier are near to some base (radix) power.

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