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Simulation Results of Combinational Circuits Using Reversible Decoder in Xilinx

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Abstract *– Reversible logic is the emerging field for analysis in present era. The aim of this paper is to appreciate differing kinds of combinational circuits like full-adder, full-subtractor, multiplexer and comparator using reversible decoder circuit with minimum quantum value. Reversible logic is extremely a lot of in demand for the long term computing technologies as they are known to supply low power dissipation having its applications in Low Power, Quantum Computing, nanotechnology, and Optical Computing. Adders and multipliers are basic building blocks in many procedure units.*

Keywords*: Quantum Cost, Reversible Gates, Garbage Outputs, Number of Gates.*

I. Introduction

The impact of very large Scale Integration (VLSI) circuits in trendy life is often seen in numerous electronic facilities. Over the years, growth within the quality of VLSI style has modified designer to include well over a million transistors on every chip. Designers are faced with the daunting task of packing a lot of practicality into a smaller space and creating a circuit that operates faster than the previous generation. Style Automation (DA) technique play a useful role during this advanced method.

In this era of technology and advancement power consumption has become a very important issue of thought. during this paper we've reduced the power consumption of 4 to 16 decoder by exploitation reversible logic. Reversible logic finds its application in quantum computing, nanotechnology, low power VLSI. within the irreversible logic for the loss of every bit of data [1] projected that KTlog2 joules of energy is dissipated, wherever K is Boltzmann‟s constant and T represents temperature. This quantity of heat is extremely small in simple circuits however it becomes massive in complicated circuits. bennett [2] describes that if all the computation is administered in reversible manner, the facility dissipation because of loss of bit are often avoided. Reversible logic involves the utilization of reversible gates that have same range of inputs and outputs and they may be made to run in backward direction additionally. every input within the circuit is related to some energy. If somewhat is lost that's range of bits at the output are less as compared to the inputs, then energy associated with the corresponding bit is dissipated within the variety of heat. Since in reversible circuits no bit loss is there thence ideally in reversible circuits no power dissipation happens. However much some power dissipation will occur, which is way but the conventional logic. The additional output utilized in order to form inputs and outputs equal are known as garbage outputs. The circuit ought to be designed in such a manner thus on keep these outputs minimum. But in sure reversible circuits constant inputs are used. These constant inputs are set either to logic one or logic 0 depending upon the operation of the circuit. Reversible gates take issue from the traditional logic gates in terms of higher than 2 factors.

Reversible logic [8] may be a very prospective approach of logic synthesis for power reduction in future computing technologies. During a reversible circuit, the amount of inputs and outputs are same and there's a one-to-one mapping between input values and output values. Reversible circuits are made exploitation reversible gates. Reversible logic plays an extensively necessary role in low power computing because it recovers from bit loss through unique mapping between input and output vectors. No bit loss property of reversible circuitry results less power dissipation than the standard one [7]. Moreover, it's viewed as a special case of quantum circuit

as quantum evolution should be reversible [7]. Over the last 20 years, reversible electronic equipment gained outstanding interests within the field of DNA-technology [7], nano-technology [7], optical computing [6], program debugging and testing [7], quantum dot cellular automata [7], and discrete event simulation [7] and within the development of extremely efficient algorithms.

II. Basic Concept of Reversible Logic

A circuit/gate is said to be reversible if the input vector is uniquely recovered from the output vector and there's a matched correspondence between its input and output assignments. Additional precisely, a reversible gate could be a k-input, k-output (denoted k*k) device that maps every possible input pattern into a novel output pattern. The inputs that assume value "0" or "1" throughout the operation are termed as constant inputs. On the opposite hand, the quantity of outputs introduced for maintaining reversibility is termed garbage outputs. Some basic reversible gates most of the nowadays used are Peres Gate (PG), Toffoli Gate (TG), Fredkin Gate (FRG), Feynman Gate (FG), changed Fredkin Gate (MFRG), BVF GATE, Double Feynman Gate (F2G) etc. From these gates MFRG and BVF gate is 4x4 gates, FG in 2x2 gates and different one are 3x3 gates. the price of reversible gate is given in terms of range of primitive reversible gates required to appreciate the circuit. [6].

II.1. Quantum Cost

The Quantum Cost of the circuit is considered by knowing the number of simple reversible gates (gates of which rate is previously identified) needed to realize the circuit.

II.2. Garbage Output

The output of the reversible gate that is not used as a main output or as input to other gates is called the garbage output. In little the unexploited output of a reversible gate (or circuit) is the garbage output (s). These garbage outputs are required in the circuit to retain the reversibility concept.

III. Proposed Methodology

The Reversible Logic involves the utilization of Reversible Gates consists of a similar range of inputs and outputs i.e., there ought to be one to 1 mapping between input vectors and output vectors. And that they is created to run backward direction additionally. In Reversible logic using outputs we will acquire full information of inputs. Reversible logic conserves data. Some price metrics like Garbage outputs, range of gates, Quantum price, constant inputs are wont to estimate the performance of reversible circuits. Garbage outputs are the additional outputs that help to form inputs and outputs equal so as to maintain reversibility. the planning of various combinatory circuits like binary comparator, Full adder, Full subtractor, multiplexer circuits using Reversible Decoder is planned with optimum Quantum price.

The multiplication is one among the useful operations. Therefore, developing a signed multiplier circuit is important. Throughout this work, we've planned Wallace reversible signed multiplier circuit by Toffoli gate (TG), Peres gate (PG), and Hagh parast-Navi gate (HNG).We enforced basic traditional reversible cells in Xilinx tool and used them inside the design of Wallace reversible signed multiplier.

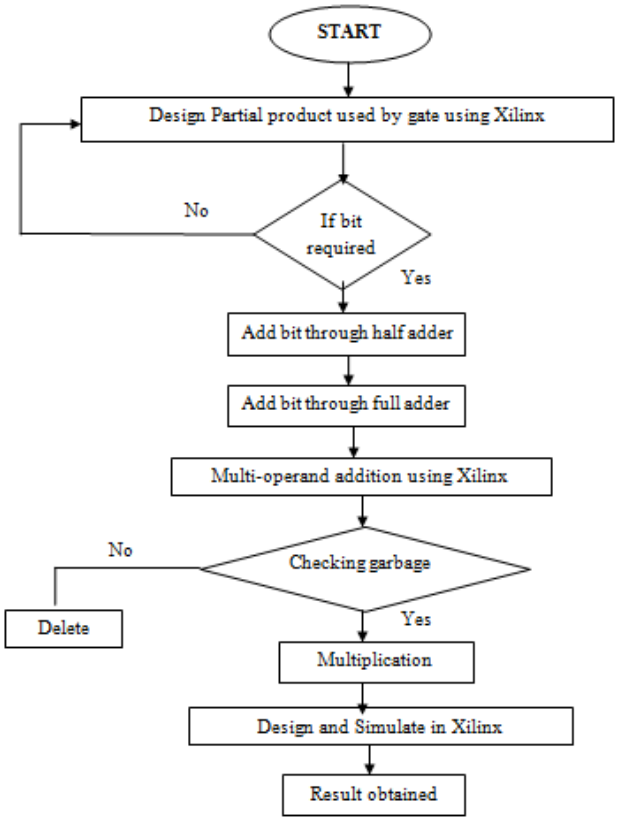

Fig.1 Flow chart of proposed work

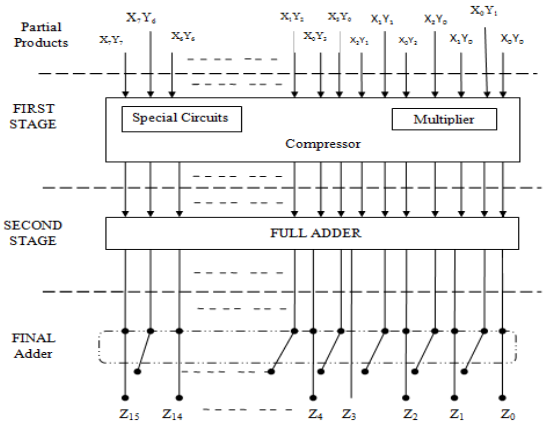

Fig.2 Block Diagram of Proposed Wallace Tree Multiplier Circuit

In his figure 2 shows the diagram of planned Wallace tree multiplier. During this diagram there 2 stage operations. Within the initial stage used special circuit, compressor and multiplier. Within the eight stage used is full adder. During this seven partial product are generate from x0y0……x7y7. The Wallace tree construction technique (as shown in Fig. 2) is used to add the partial product throughout a tree-like fashion therefore on supply 2 rows of partial product which will be other among the last stage. Although fast, since its essential path delay is proportional to the logarithm of the quantity of bits among the multiplier, the Wallace tree introduces totally different issues like wasted layout space and increased quality. Among the last stage, the two-row outputs of the tree are other using any high-speed adder like carry save adder to induce the output result. In contrast to the quality Wallace tree multiplier factor, an economical high speed Wallace tree multiplier consists of compressor adders and changed carry choose adder [4]. throughout this style, 4:2 and 5:2 compressors are used for partial product reduction inside the second section whereas carry select adders are used to perform addition of two rows of bits inside the top for reduction in carry propagation latency of the Wallace multiplier.

IV. Simulation Results

This module is implemented on Xilinx software. In this the module Wallace tree multiplier circuit implemented on Xilinx 14.1. We are using Spartan3E – XC3S100E FPGA family for designing the Wallace tree multiplier circuit with 5VQ100 package and the simulation process is also designing by Xilinx simulation tools known as Modelsim simulator.

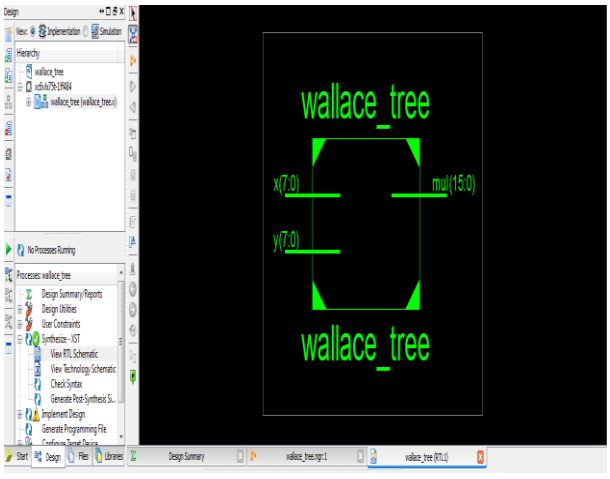

Fig.3: Top Level Hierarchy of Wallace tree

This fig.3 shows the top level of Wallace tree multiplier. In this two input and one output. That is two inputs is 8 bit number multiplicand and 8 bit number multiplier then output is 16 bit multiplier.

This fig.4 shows the RTL schematic of Wallace tree multiplier circuit. In this architecture used of number of LUTs, number of different compressor and number of I/OBs.

This fig.5 shows simulations results of Wallace tree multiplier. In this simulation give two 8 bit numbers input and get the 16 bit output. And get also sum and carry.

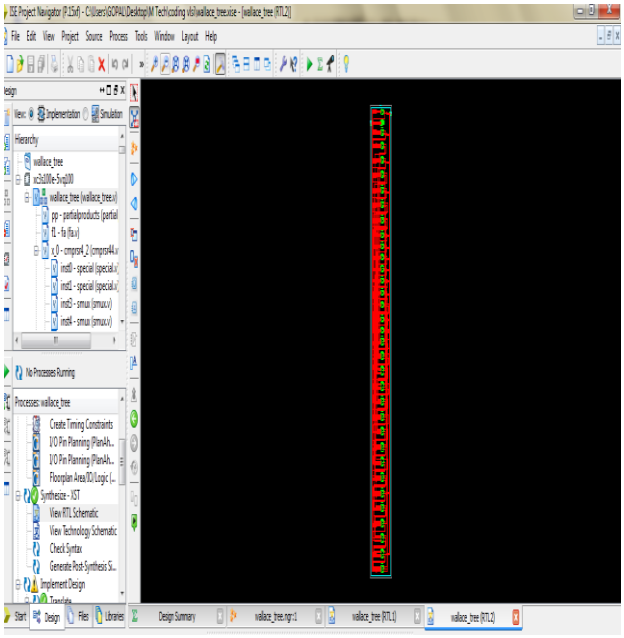

Fig.4 RTL Schematic of Wallace Tree Multiplier Circuit

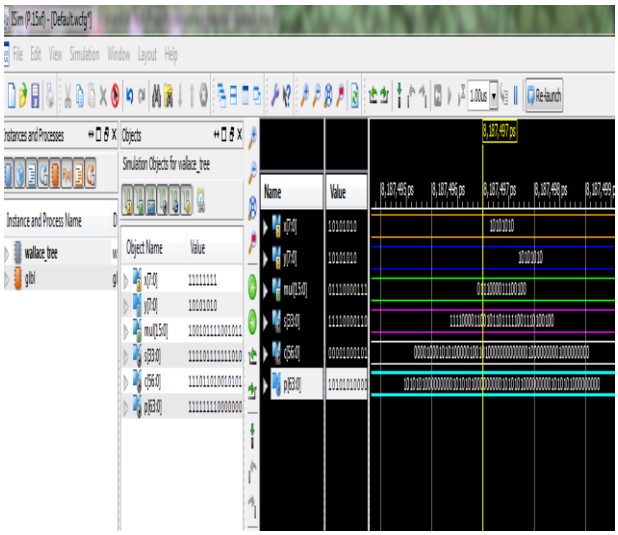

Fig.5: Simulation Result of Wallace Tree Multiplier Circuit

V. Conclusion

The planned multiplier factors are over the current designs due to reducing the amount of gates, garbage

outputs, hardware complexness and sort of transistors required. The ability dissipation of reversible logic style over irreversible logic style is low. Our planned reversible multiplier circuit is applied to the look of difficult systems in nanotechnology. The planned Wallace reversible multiplier circuit is best than the current styles in terms of hardware quality, sort of gates, garbage outputs and constant inputs. The implementation of planned reversible logic multiplier circuit exploitation 8X8 wallace tree Techniques that has 2 main features: One is implementing the multiplier exploitation reversible logic will increase the speed of the multiplication and second is the use of 8X8 wallace tree Techniques reduces the world and also the hence the power dissipation.

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