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Low-Power Near-Threshold 10T SRAM Bit Cells With Enhanced Data-Independent Read Port Leakage for Array Augmentation in 32-nm CMOS

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Abstract- In a ultralow voltage operation of Digital Circuits will improve the performance in all application with high constraints, energy efficiency and low power consumptions. In this area memory system will take major role to storing and retrieving data with using SRAM memory cells. This SRAM will have lot of complexity in Write and Read operations due to more number of Transistors, thus it will choose column and row selection method. In this proposed work will hybrid two single ended (SE) differential SRAM for write and read operation to reduced the hardware complexity and power consumption, for write operation 6T SRAM will used and for read operation 4T SRAM will used, it will take totally 10T SRAM. This technique is adopted using differential VDD technique to improved write ability of the design. Further the proposed architecture will designed up to 8-Bit 10T SRAM cell to test and proved the efficiency. Finally this work will developed in Tanner EDA using 45nm CMOS Technology with 1V supply voltage and proved the comparisons with existing 65nm CMOS Technology in terms of area, delay and power.

Keywords : SRAM,SE10T SRAM, 45nm, Power optimization, Area optimization

I. Introduction

SRAM contributes to the major portion of SoCs. The portables devices often require stable, low power SRAMs [1]. There is a growing trend to implement SoC based applications using FPGA due to its reconfigurability and prototyping [2]-[3]. There is a huge necessity for the on-chip memory for these FPGA implementations. SRAM is suitable for its faster response for cache memory [4]. Applications like Wireless Sensor Networks (WSN), biomedical devices often require low power. WSN offers a wide range of services like establishing the connection, transfer of information and gathering of data for conventional internet usage and industrial internet. WSN consists of sensor nodes. They communicate with the end-user using gateway which uses internet protocol to link sensor nodes and IP network. As multiple wireless sensor nodes form WSN in a particular remote area, longer battery life is often needed which reduces the burden on humans to replace the batteries every time. So lower power consumption is necessary for SoC using IoTs [5]. With the usage of IoT in the digital health system, Body Sensor Networks (BSN) are widely used. BSN consists of different sensors which monitor the physiological signals from a person [6]. The data, which was monitored, is sent to the nearest medical center for examination through the base station. The BSNs which process and store the data, often require memory to store it before transmitting to the medical center. SRAM plays a vital role in such applications due to its speed response. Portable devices, to enhance their performance, use embedded SRAM as a cache that uses FPGA to realize the digital systems [7]. SRAM design is used to store 1-bit of data. So, SRAM cell is used for FPGA devices. The LUT in FPGA stores the truth table. It is a table that maps to an output for the respective inputs. LUT is realized using SRAM cells. LUT forms the major building block of FPGA, which is realized using SRAM cells. So, decrease in leakage power of SRAM cell will ultimately reduce the overall leakage power of FPGA. With the scaling of technology nodes on the rise, the leakage power consumption is higher than that of the overall power consumption. Many of the SRAM cells for a greater amount of time operates in hold or standby mode [8]. So low leakage power is a significant parameter that needs to be reduced. Leakage currents contribute greater than 40% of active power in SoCs with enhanced performance [9]. So low leakage power is a significant parameter that needs to be reduced. Techniques like operating in subthreshold region, reduction in VDD in idle mode, usage of multi-threshold devices and power gating [10]-[12] can reduce the active as well as the leakage power. However, reduction in VDD leads to declined stability, prone to Process-Voltage-Temperature (PVT) variations.

The demand for portable applications such as mobile phones, laptops, and medical devices like pacemaker, defibrillator, and pedometer require ultra-low power in integrated circuits. Low power static random access memory (SRAM) is particularly important because of a major portion of the system on chip is occupied by them [1]. Supply voltage scaling is one of the popular techniques to reduce power consumption [2]. The scaling of supply voltage reduces both leakage and dynamic powers. Many researchers have designed logic circuits in the sub-threshold region to gain the benefits of the supply voltage scaling scheme. However, MOSFETs undergo short channel problems in scaled technologies, especially in the sub-threshold region, which also leads to increased sensitivity to process variation in these devices [3].

Furthermore, the scaling of supply voltage degrades the performance [4]. As technology entered into the sub-100 nm regime, threshold voltage, leakage current and process, voltage and temperature (PVT) variations are of serious concern. Static noise margin degrades linearly as the supply voltage is scaled down because it has an exponential relationship with threshold voltage [5]. So it is challenging to maintain the cell stability and therefore, read and write failure probabilities are considerably increased in the conventional 6T SRAM under lower supply voltages [6]. Many SRAM cell designs have been proposed in the literature, solving one or multiple challenges mentioned above [7–9]. Some techniques reported for improving write noise margin are – WL boosting [10], power cut-OFF [11], raising the cell Vss [12], and negative bit-line (NBL). Another approach to improve read stability is the use of a separate path for reading operation. This read decouple technique enhances the read stability at a cost of extra transistors [13, 14]. Moreover, energetic alpha particles, neutrons, cosmic rays, and protons can create disturbance in the stored data of the memory [15]. As the technology scales down, the disturbance in stored data increases [16] during a write operation in half selected SRAM cells as their WLs are activated. As a result, SRAM cells are written inadvertently [17]. Moreover, read assist circuit based SRAM faces the same problem as in half selected SRAM [18]. Consequently, SRAM cells need to be protected during the half select, otherwise, the cell may lose their data during the write operation [19].

Ultralow-voltage SRAM and logic are commonly used for powerconstrained applications, such as internet of things [1], wireless sensor networks [2], and medical apparatuses [3]. Scaling down supply voltage is a simple and effective way to reduce energy, but the excessive pursuit of near-threshold operation will increase the process variability and degrade the reliability of system. Fig. 1 shows the normalized supply voltage scaling trends of the frequency and energy efficiency of SRAM and logic circuit, respectively. As VDD is scaled down into the near-threshold region, the energy efficiency per operation is significantly increased and the frequency degrades gracefully [4,5]; But as the supply voltage steps into the sub-threshold region, the frequency and the energy efficiency decreases dramatically, this is because the leakage energy dominates in this region [6]. Compared to combinational logic, the performance of SRAM degrades more significantly than logic in ultralow voltage. This phenomena occurs because the memory bit-cells has both larger process variation and higher robust requirements than logic due to its small transistor size and large capacity. To enhance the access reliability and alleviating the speed degradation of SRAM in supply voltage scaling, many assist techniques have been proposed, such like word-line boosting schemes, negative bit-line (NBL) methods, bit-cell structure enhancement and timing error detection techniques. Word line boosting schemes involve increasing the word line voltage to enhance the strength of the pass transistor, leakage power and static noise margin (SNM) of the selected bit-cells are not affected while the cell writability and readability are greatly enhanced if the write word-line and read word-line are both boosted [7,8]. However, the disadvantage of these techniques are the reduction of SNM of the unselected bit cell in the same row [9]. In NBL technique, the bit line is lowered to a negative value to increase strength of the access transistor [10,11]. The bit line voltage is pulled negative by a boost capacitance. Compared to the word line boosting techniques, the NBL technique is superior as it does not degrade the read noise margin (RNM) of the unselected bit cells [8]. But the RNM is affected for the unselected bit cell in the same column due to the increase of leakage current. Various SRAM bit-cells [12–18] have been proposed to enhance stability of SRAM cell for robust low voltage/power operation. In [12–17], asymmetric SRAM cells enhance the Read stability by weakening one-side of NMOS pull-down transistor with single Read port to mitigate Read disturb. In [18], Schmitt-trigger-based SRAM cells are formed by applying half Schmitt trigger in pull-down path of a SRAM cell.

II. RELATED WORK

Harekrishna Kumar ek.al.(1) “A Review on Performance Evaluation of Different Low Power SRAM Cells in Nano‑Scale Era” In this paper, a detailed comparative analysis of different SRAM cells has performed on the basis of various design parameters such as power dissipation, delay, area, energy and stability. It is observed that 9T SRAM cell is better in terms of read stability and read current whereas 7T SRAM cell is superior for write ability among considered topologies. Further, read and write power dissipation in 8T and 7T SRAM cell is lowest among considered topologies. In addition to this, statistical analysis of read stability, read power, read current, leakage power and leakage current has been performed with the help of Monte Carlo Simulation. This work also incorporates the overall performance of simulated topologies in terms of SAPR value. It is found to be highest in 8T SRAM cell. Hence, it can be concluded from the meticulous survey and comparative analysis performed in this paper that a SRAM cell can be designed with more robust nature by optimizing the trade-off between various performance parameters [1].

Pan Yang ek.al.(2) “An error detecting scheme with input offset regulation for enhancing reliability of ultralow-voltage SRAM” The ED-SA scheme is proposed to eliminate the extra design margin caused by the weak bit cells and detect the error bits in ultralow-voltage SRAM design. Simulation results show the proposed error detect technique has a notable reading yield and reliability improvement under ultralow voltage range. Compared

with the previous error detecting SRAM, the reading yield of the proposed technique achieves 1.24 × −7× improvement in 512 × 32 array organization [2].

Rohit Lorenzo ek.al.(3) "Single bit-line 11T SRAM cell for low power and improved stability" In this paper, a half-select free-based new 11T SRAM cell is presented. The proposed cell removes read disturbance and improves the write-ability by cutting-OFF the path from the power sources to storage nodes. The proposed cells consume less power dissipation as compared to the other SRAM cells because of the elimination of unnecessary BL discharges, stacked transistor, and VGND control. The cell also exhibits less write delay as compared to other SRAM cells because of access TG. We have seen the usefulness of the P11T SRAM cell under various PVT variations. So the P11T cell is an attractive choice because of its several advantages [3]Zhiting Lin ek.al. (4) "In-Memory Computing With Double Word Lines and Three Read Ports for Four Operands" To resolve the bottleneck of the traditional von Neumann architecture, we propose an 8T cell array with separated write lines (WLL and WLR) to perform four-input logic operations and CAM functions without modifying the transistor size. The redundant column is used to generate the reference voltages. Furthermore, the performance of the proposed scheme is evaluated under the worst condition. The operation frequency is 505 and 813 MHz at 1 and 1.2 V, respectively. It achieves 0.24 fJ/search/bit at 0.6 V. The proposed scheme can be used for in-memory computing logic operations, such as a Hamming code, which is significant for the error correction [4]. Lu Lu ek.al (5) "A 0.506-pJ 16-kb 8T SRAM With Vertical Read Wordlines and Selective Dual Split Power Lines" In this article, a 16-kb 8T SRAM array with vertical RWL and SDSP for ultralow-power applications has been presented. The column-based RWL reduces the dynamic energy consumption by only discharging the selected RBL in one column MUX (CMUX). A single-ended write operation is developed with vertical control. Finally, the proposed data-aware SDSP enhances WM and SNM simultaneously. The test chip of the proposed SRAM is fabricated in 65-nm CMOS technology. Based on the experimental result, the minimum energy per bit of 31 aJ is achieved at 0.4 V. This achieves the smallest normalized energy per bit when compared to other state-ofthe- art works. The SRAM is successfully functional down to 0.26 V [5]. Soumitra Pal ek.al. (6) "Reliable write assist low power SRAM cell for wireless sensor network applications" In this work, a reliable WALP11T SRAM cell has been proposed. In order to improve the read stability a read decoupling technique has been used. The write ability of the cell is significantly improved due to the presence of multiple charging and discharging paths during the write operation, as VSSL and VSSR are kept at VDD or GND depending on type of write operation. In the standby mode, both VSSL and VSSR are kept at VDD, to curtail bitline leakage. For further reduction of static power dissipation, an additional tail-transistor, MN9, is stacked with the cross-coupled inverter. Upon comparison with other cells, the proposed cell exhibits improvements in terms of major design metrics analysed under considerable process variations. Furthermore, the WALP11T cell functions reliably even when operating in extreme process corners and takes up lesser area than that of WWL12T and D12T cells. Thus, the proposed WALP11T cell, is an optimum choice for robust and power-efficient cache memory design for WSN applications [6]. Prakhar Sharma ek.al. (7) "A Single-Ended 10-Transistors Static Random Access Memory Bit-Cell With Improved Write- Margins at Low Voltages and High ION-IOFF Ratio" In an attempt to prevail over the challenges faced by conventional bit-cells, a single-ended '10T' bit-cell is proposed in this paper. The bit-cell is equipped with two supplementary pMOS transistors in its latch which aid in improving the write margins of the bit-cell even at low voltages. The bit-cell is then compared with conventional SRAM bit-cells on the basis of various performance metrics at 32 nm technology at a voltage range varying from 0.3V to 1V. The write-ability improvement technique employed in the '10T ' bit-cell is observed to allow up to 1.27 and 1.30 higher write margins when compared with '8T ' and '6T ' bitcells respectively. It is also observed that the '10T' b it-cell retains its hold stability by 83.46 mV at 0.4V even in the half-selected state when the write operation is performed on a bit-cell in the same column. In the read port, VVSS reduces the bit-line leakage current by up to 67.01 when compared with the read port of '8T' bit-cell. The higher ION-IOFF ratio of the '10T' bit-cell allows greater number of bit-cells to be supported by the read bit-line when the read operation is performed [7].

III. Method

In Memory system, SRAM plays major role in storing bit .but for low voltage applicaton SRAM gives loss in both area and power. And they suffered from Bit Interleaving (column selection).In this proposed SE -10T SRAM is designed for supporting Bit Interleaving and also for power reduction. In addition featuring bit line-shared data-aware write assist to enable the column-selection structure . Further here 8 bit 10T SRAM also designed and implemented. Compare to the existing method, the proposed design have more power reduction and area size. Finally, the proposed design is implemented in the TANNER EDA at 45nm CMOS Technology with 0.9V input voltage and proved the comparison in terms of area power and delay.

The original SE-10T SRAM cell of the proposed bit cell is shown in Fig. .1. A 4T read port composed of an inverter and a transmission gate (TG) is added to the 6T cell, isolating the read path from internal storage nodes. The inverter (M6 and M7) is driven by node QB and drives the read bit-line (RBL) through TG (M8 and M9) which is controlled by two complementary read word lines (WLs). This SE-10T cell can fully charge or

discharge RBL by itself during a read operation. Thus, it is totally unnecessary to prepare a pre-charge circuit for RBL. The dynamic power is consumed on RBL just when the read datum is changed. That is to say, the dynamic power dissipation on RBL is zero if consecutive "0"s or consecutive "1"s are read out. This feature makes it suitable for video processing since image data have the special correlation, and similar data are read out in consecutive cycles [11]. Unfortunately, due to its 6T-like write operation, when initiating a write in a column-selection array, unselected cells in a row (or called half-selected cells) on the selected WL perform dummy read which indicates that the cells just undergo a read behavior rather than readout during a write operation, thereby experiencing the storage node upset similar to read disturb in the 6T cell. In other words, it is not eligible for the bit-interleaving architecture. In addition, the full rail-to-rail swing occurred on RBL congenitally dissipates more power compared with the differential readout. Meanwhile, bitlines incur more leakage current because of TG.

This SE-10T cell has been presented in [11]. However, our proposed 10T (thereafter called P-10T) circuit topology is different from the earlier design. Fig. 4.1 shows the P-10T based on the SE-10T cell. It exhibits improvements in the following aspects compared with the previous circuit.

First of all, the bitline-shared data-aware scheme is adopted to enable the column-selection architecture. In Fig. 2, the 6T part of the SE-10T cell is motivated by the y-direction (column direction) WL [column WL (CWL)]. In addition, two additional access transistors (M10 and M11) are added to connect the 6T cell, which

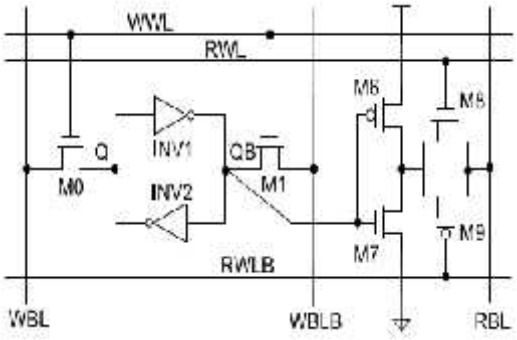


Figure 1: Schematic of Proposed SE-10T SRAM.

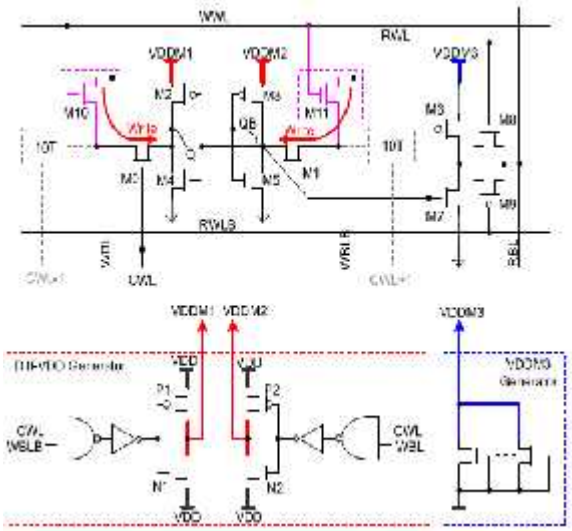


Figure 2:Proposed SE-10T SRAM with assist circuit.

are activated by the x-direction (row direction) write WL (WWL) and at the same time are powered by a complementary write bit line pair (WBL and WBLB). Every extra access transistor and write bit line are shared by two adjacent 10T cells in a row. During a write operation, the data are written into the storage core from shared write bit lines via shared access transistors and internal access transistors, just when row WL and column WL are all switched ON. The proposed bit-interleaving-enabled scheme is different from the previous design in [12] where the SRAM array is also able to be column-interleaved by vertical and horizontal WLs. Nonetheless, its write access devices are shared by several bit cells in a column, whereas the write access ones are shared by two bit cells in a row in our design.

Diff-VDD Write Assist

The proposed design utilizes the row and column coordination modes of WLs to eliminate the half-selection problem, which leads to the degradation in the write ability due to the series-connected write access n MOSs just like in the Diff-10T cell. This could be highly problematic, particularly in the slow nMOS fast pMOS (SNFP) corner, where the driven strength of nMOS is less than that of pMOS. To solve this issue, the Diff-VDD scheme (shown in Fig..2) is presented. Fig. 4 shows the write waveforms of the cell to describe the write assistant circuit how to work.

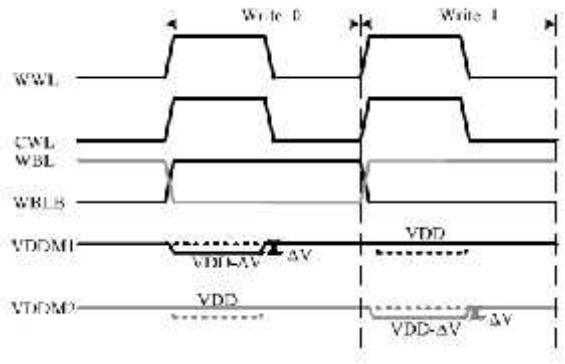


Figure 3: Write waveform of proposed cell.

Generally, VDDM1 and VDDM2 are all equivalent to VDD because the pMOSs P1 and P2 in the Diff-VDD generator (4.4) are both turned on (CWL = 0). During a write "0" operation, WLs WWL and CWL are

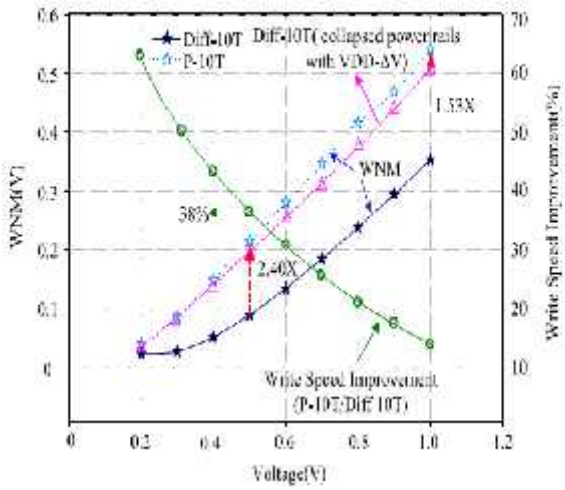


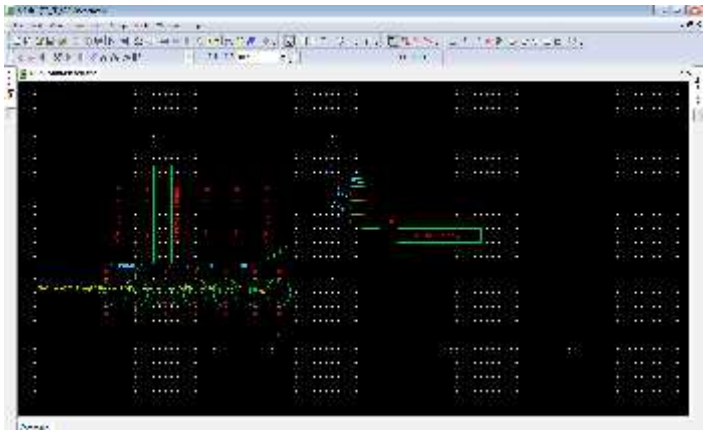
Figure 4: the comparison of WNM and write speed of the cells

turned on, while bit line WBL is set to low and WBLB goes to high. Subsequently, the nMOS N1 is ON (CWL and WBLB = 1), resulting in a V voltage drop on VDDM1. At this time, VDDM2 resides at VDD since CWL AND ing WBL equals 0. The dropped VDDM1 is able to attenuate the pullup strength of pMOS M2 effectively, making the cascaded access n-MOSs M0 and M10 absolutely pull the storage node Q down to "0." Under the same condition, WBL goes to high, and WBLB is driven to low initiate a write "1" behavior. Similarly, a reduction of V on VDDM2 power rail (CWL and WBL = 1) undermines the pull-up strength of pMOS M3 to ensure that the node QB can be discharged to "0" definitely by M1 and M11. The proposed Diff VDD exerts a prominent advantageous impact on the write ability, facilitating the write operations.

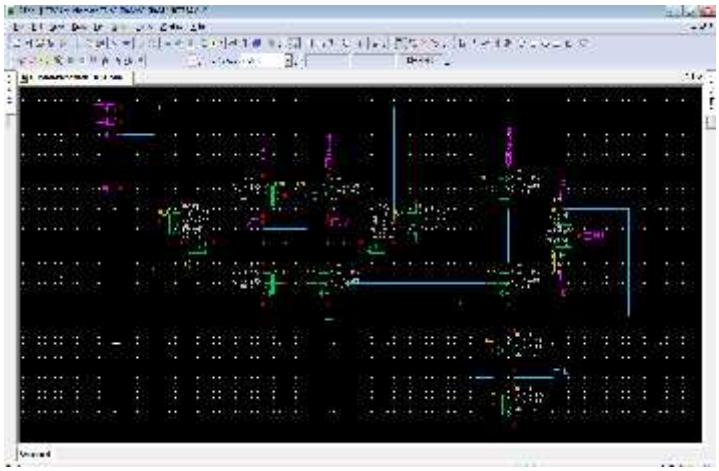
IV. Simulation Results

In this section show implementation result using Xilinx and Modelsim for SRAM analysis and shows their parameter.

10T SRAM:



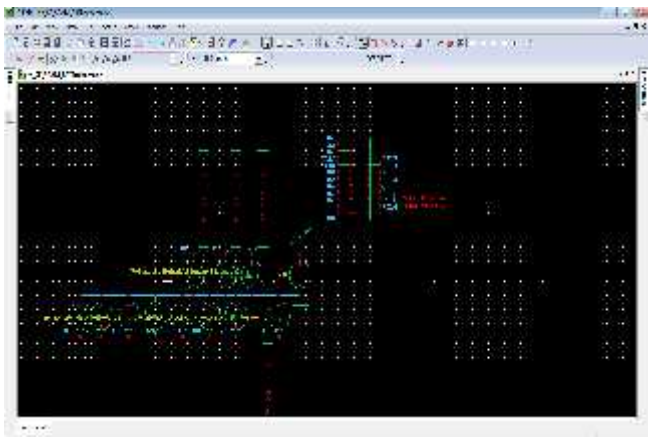
(A) Top View



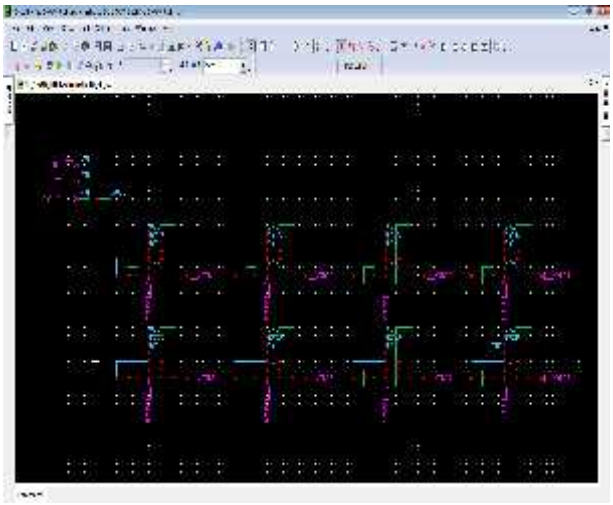
(B)Inner Architecture

Figure 5: SRAM 10T Diagram

Figure 5 is show SRAM 10T Architecture. A is show top view of design and B is inner architecture.



(A) Top View



(B) Inner Architecture

Figure 6 :10T SRAM FOR 8 BIT

Figure 6 is show SRAM 10 8 bit architechture.

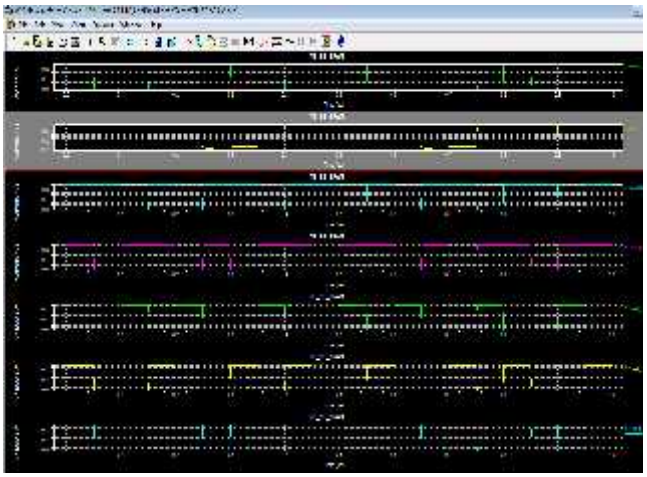


Figure 7: W-edit output

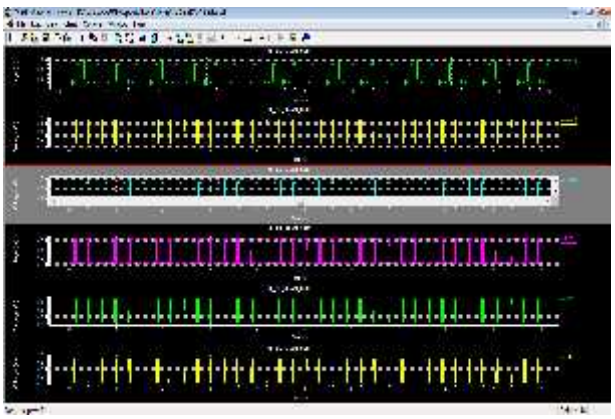


Figure 8: Simulation Output

Table 1 Parameter Compare For SRAM 10 T

	Column-Selection-Enabled 10T SRAM Utilizing Shared Diff-VDD Write and Dropped-VDD Read for Power Reduction			
	SE-10T SRAM (1-Bit)		SE-10T SRAM (8-Bit)	
	CMOS 65nm	CMOS 45nm	CMOS 65nm	CMOS 45nm
MOSFET	33	33	282	282
Area(mm)	2.145	1.485	18.33	12.69
Power(uW)	62.25	69.7	9.45	1.915

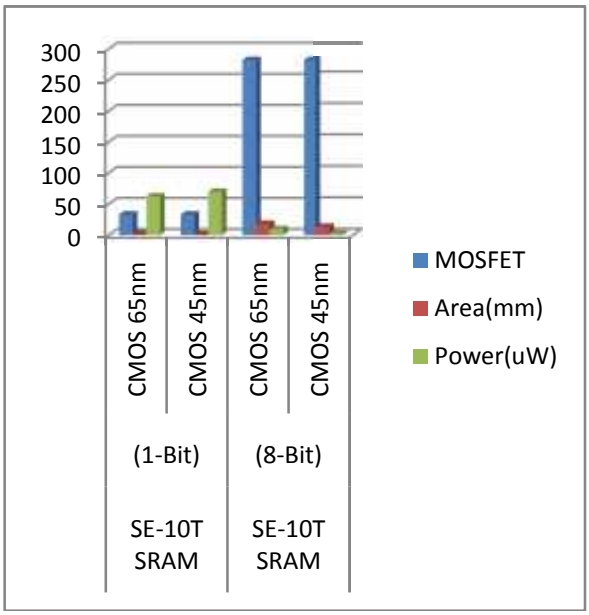


Figure 9: Parameter compares graph

V. Conclusion

From proposed methodology we are design SE-10T RAM. This SRAM will have lot of complexity in Write and Read operations due to more number of Transistors, thus it will choose column and row selection method. In this proposed work will hybrid two single ended (SE) differential SRAM for write and read operation to reduced the hardware complexity and power consumption, for write operation 6T SRAM will used and for read operation 4T SRAM will used, it will take totally 10T SRAM. This technique is adopted using differential VDD technique to improved write ability of the design. Further the proposed architecture will designed up to 8-Bit 10T SRAM cell to test and proved the efficiency.

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