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A Novel Logic Style Used For Leakage Power Reduction in MOS Integrated Circuit

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Abstract *– Full adders are necessary parts in applications corresponding to digital signal processors (DSP) architectures and microprocessors. Additionally to its main task, that is adding 2 numbers, it participates in several different helpful operations appreciate subtraction, multiplication, division, address calculation, etc. In most of those systems the adder lies in the critical path that determines the general speed of the system. Therefore enhancing the performance of the 1-bit full adder cell (the building block of the adder) could be a significant goal. Demands for the low power VLSI approaching the expansion of insistent design process to control use severely. To accomplish the rising demand, we advise a new low power adder by give up the MOS transistor calculate that reduce the grave threshold defeat so anew enhanced 14T CMOS l-bit full adder cell is specified in this paper. Results show five hundredth improvement in threshold loss drawback, 45% improvement in speed and considerable power consumption over the given adder and other different types of adders with comparable presentation.*

Keywords*:* Arithmetic circuit, full adder, multiplier, low power, very Large-scale integration (VLSI).

I. Introduction

ADDER

In practically all digital Integrated Circuit designs today, the addition procedure is one of the mainly necessary and frequent procedures. Instruction set for DSP's and all-purpose reason processors consist of at least one category of addition. Other commands like subtraction and multiplication make use of addition in their procedure and their underlying hardware is alike if not equal to addition hardware. Often, an Adder or multiple adders will be in the critical path of the preparation, hence the management of a recommend Will be often be limited by the performance of its adders.
When the designers look at further element of a chip, such as region or control, will find that the Hardware for addition will be a large contributor to these areas. It is then of assistance to choose the correct adder to implement in a design for the reason that the many feature it aspects in the overall chip.

TYPES OF ADDER

In this section we have reviewed several types of adders and studied their operation and performance. The various types of adders are:

- Basic Adder Units
- Half adder
- Full adder
- Parallel Adders
- Ripple carry adder
- Carry look ahead adder

A. BASIC ADDER UNITS

i. HALF ADDER

A combinational circuit that adds two bits is known as a half adder. The half adder adds two single A and B Binary digits has two outputs, sum (S) and carry (C). With the combinational of an OR gate to join their carry outputs, two half adders be able to combined to create a full adder. Equations are the Boolean equations for sum and carryout.

$$Sum = a \oplus b \quad (1)$$

$$Carry = a \cdot b \quad (2)$$

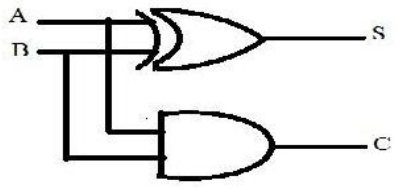

Figure 1.1: Gate Schematic for Half Adder

ii. FULL ADDER

A full adder join three bits, the third bit produced from a preceding addition operation. A full adder

combine binary figures and accounts for values carried in as well as out. A one-bit full adder join three one-bit numbers, frequently written as A, B, and Cin; operands are A and B, and Cin is a bit carried in from the next less considerable step.

$$S = A \oplus B \oplus Cin \quad (3)$$

$$Cout = (A \cdot B) + (Cin \cdot (A \oplus B)) \quad (4)$$

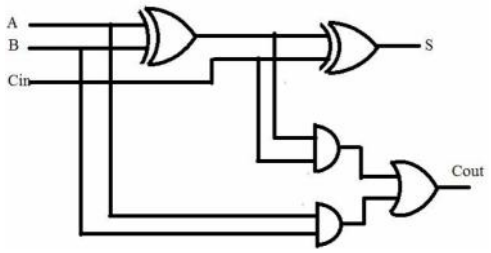

Figure 1.2: Schematic symbol for a 1 bit FA

B. PARALLEL ADDER

i. RIPPLE CARRY ADDER

The Ripple Carry Adder is the simplest adders to put into practice. This adder takes two inputs of N-bit and give (N+1) output bits The RCA is create from N full adders which are cascaded together, with the carryout bit of one Full adder coupled to the carryin bit of the next Full Adder. The input bits are labeled a and b, the carryout of each Full adder is labeled sum and the cout bits are labeled sum. Every sum bit needed both input and Cin prior to it can be calculated. From a VLSI design viewpoint, this is the easiest adder to put into practice. One just require to design and layout one Full Adder cell, and then array N to create an N-bit RCA of of these cells. The performance of the one Full Adder cell will chiefly find out the speed of the entire RCA.

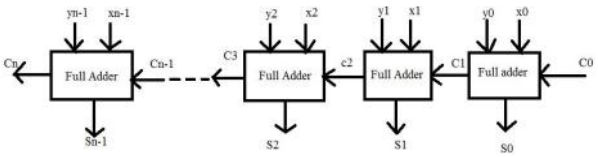

Figure 1.3: Schematic for an N-bit Ripple Carry Adder

ii. CARRY LOOK AHEAD ADDER

The Carry Look Ahead adder utilizes partial full adders as explain in equation to estimate generate and broadcast signals required for the carryout equations. Smith and Weinberger discovered the Carry Look Ahead Adder. The equations for c2, c3 and c4 are attained by substitution of c1, c2 and c3, correspondingly. These equations explain that each carryout in the adder can be find out with just the input operands and initial carryin. This procedure of calculating ci by with only the pi, gi and c0 signals be capable of to be done indefinitely, on the other hand, each subsequent carryout produced in this manner becomes more and more difficult as the large number of high fan-in gates .

$$c_1 = g_0 + p_0.c_0 \quad (5)$$

$$c_2 = g_1 + p_1.c_1 = g_1 + p_1.g_0 + p_1.p_0.c_o \quad (6)$$

$$c_3 = g_2 + p_2.c_2 = p_2.g_1 + p_2.p_1.g_0 + p_2.p_1.p_0.c_0 \quad (7)$$

$$c_4 = g_3 + p_3.c_3 = g_3 + p_3.g_2 + p_3.p_2.g_1 + p_3.p_2.p_1.g_0 + p_3.p_2.p_1.p_0.c_0 \quad (8)$$

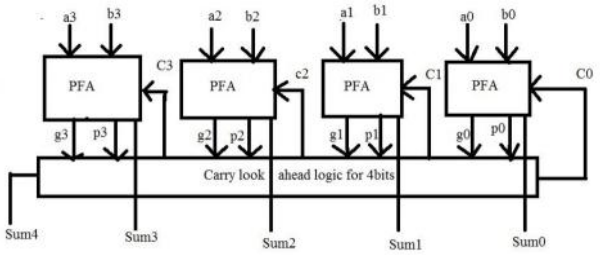

Figure 1.4: 4-bit carry look-ahead adder

II. Literature Survey

Jatin N. Mistry et.al.[1] "Active Mode Sub clock Power Gating" The proposed technique achieves power reduction through two mechanisms: 1) power gating the combinational logic within the clock period (sub-clock) and 2) reducing the virtual supply to less than Vth rather than shutting down completely as is the case in conventional power gating. To achieve this reduce voltage, two sets of experiments are done: the first experimentally validates the functionality of the proposed Technique in the fabricated test chip and the second investigates the utility of the proposed technique in example applications. Measured results from the fabricated chip show 27% power saving during the active mode for an example wireless sensor node application when compared to the same microprocessor without sub-clock power gating applications. This paper has proposed a power gating technique that reduces leakage power during the active mode for low performance energy constrained applications by power gating combinational logic within the clock period. Rather than
Shutting down completely, symmetric virtual rail clamping was proposed to reduce wake-up power mode transition energy cost. The proposed sub-clock power gating with symmetric virtual rail clamping technique has been demonstrated with an ARM Cortex-M0 microprocessor, fabricated in 65nm technology.

H. J. M Veendrick et.al.[2], "Short circuit dissipation of static CMOS circuitry and its impact on the design of buffer circuits ," This paper gives a detailed discussion of

the short-circuit component in the total power dissipation in CMOS circuits, on the basis of an elementary CMOS inverter. Design considerations are given for CMOS buffer circuits, based upon the results of the dissipation discussion, to increase circuit performance. A detailed discussion of this short circuit dissipation is given based upon the behavior of the inverter when loaded with different capacitances. It was found that if each inverter of a string is designed in such a way that the input and output rise and fall times are equal, the short-circuit dissipation will be much less than the dynamic dissipation (<20 percent). This result has been applied to a practical design of a CMOS driving circuit (buffer), which is commonly built up of a string of inverters. An expression has also been derived for a tapering factor between two successive inverters of such a string to minimize parasitic power dissipation. Finally, it is concluded that optimization in terms of power dissipation leads to a better overall performance (in terms of speed, power, and area) than is possible by minimization of the propagation delay.

K Roy et.al.[3], "Leakage current mechanism and leakage reduction techniques in deep-sub micrometer CMOS circuits," High leakage current in deep-sub micrometer regimes is becoming a significant contributor to power dissipation of CMOS circuits as threshold voltage, channel length, and gate oxide thickness are reduced. Consequently, the identification and modeling of different leakage components is very important for estimation and reduction of leakage power, especially for low-power applications. This paper reviews various transistor intrinsic leakage mechanisms, including weak inversion, drain-induced barrier lowering, gate-induced drain leakage, and gate oxide tunneling. Channel engineering techniques including retrograde well and halo doping are explained as means to manage short-channel effects for continuous scaling of CMOS devices. Finally, the paper explores different circuit techniques to reduce the leakage power consumption.

M. Anis et.al[4] "Dynamic and leakage power reduction in MTCMOS circuits using an automated efficient gate clustering technique," This paper presents two techniques for efficient gate clustering in MTCMOS circuits by modeling the problem via Bin-Packing (BP) and Set-Partitioning (SP) techniques. An automated solution is presented, and both techniques are applied to six benchmarks to verify functionality. Both methodologies offer significant reduction in both dynamic and leakage power over previous techniques during the active and standby modes respectively. Furthermore, the SP technique takes the circuit's routing complexity into consideration which is critical for Deep Sub-Micron (DSM) implementations. Sufficient performance is achieved, while significantly reducing the overall sleep transistors' area. Results obtained indicate that our proposed techniques can achieve on average 90% savings for leakage power and 15% savings for dynamic power. Two techniques are applied to efficiently cluster gates in MTCMOS Circuits. The first gives the minimum number of sleep transistors to be employed, while the second takes the circuit's routing complexity into consideration. On average the BP technique reduces dynamic and leakage power by 15% and 90% respectively. The SP technique also reduces dynamic and leakage power on average
by 11% and 77% respectively. Future work involves improving the computation time involved to solve the SP and BP problems by using heuristic search techniques in the form of Genetic Algorithms that are suitable for multi-objective optimization problems.

R. Gonzalez,et.al.[5]"Supply and threshold voltage scaling for low power CMOS," — this paper investigates the effect of lowering the supply and threshold voltages on the energy efficiency of CMOS circuits. Using a first-order model of the energy and delay of a CMOS circuit, we show that lowering the supply and threshold voltage is generally advantageous, especially when the transistors are velocity saturated and the nodes have a high activity factor. In fact, for modern submicron technologies, this simple analysis suggests optimal energy efficiency at supply voltages under 0.5 V. Other process and circuit parameters have almost no effect on this optimal operating point. If there is some uncertainty in the value of the threshold or supply voltage, however, the power advantage of this very low voltage operation diminishes. Therefore, unless active feedback is used to control the uncertainty, in the future the supply and threshold voltage will not decrease drastically, but rather will continue to scale down to maintain constant electric fields. We found the supply and threshold voltages for optimal EDP using a first-order model of energy and delay in CMOS circuits that take into account leakage current. The location of this point and the shape of the EDP surface near the minimum are a strong function of how velocity-saturated the transistors are. If transistors are not velocity-saturated then the EDP surface is relatively flat. As transistors become more velocity-saturated, the EDP surface becomes steeper and the optimal point moves closer to the origin. For a 0.25- m technology, this analysis yielded a supply of 250 mV and of 120 mV. One difficulty with operating at this point is that the speed of each gate is modest, forcing the designers to reduce the levels of logic in their design to maintain performance In order to achieve the large potential gains of operating at low voltages, the circuit needs to use some kind of adaptive control on both the threshold voltage and the supply, to reduce the effective variation that the circuit sees. Until energy efficient techniques are developed to accomplish this, the supply and threshold scaling is likely to be more modest, probably at a rate that maintains constant electric fields within the devices.

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III. Method

MODIFIED CONSTANT LOGIC STYLE

Modified CD logic is created by doing 3 changes are as follow.

1. Window adjustment technique is eliminated.
2. Evaluation transistor is altered as pMOS transistor instead of nMOS.
3. Addition of transistor M2 and M3 in parallel below the pull down network.

The proposed logic helps to reduce the power and delay which in turn reduces the power delay product.
The circuit diagram for the proposed logic is shown in Fig

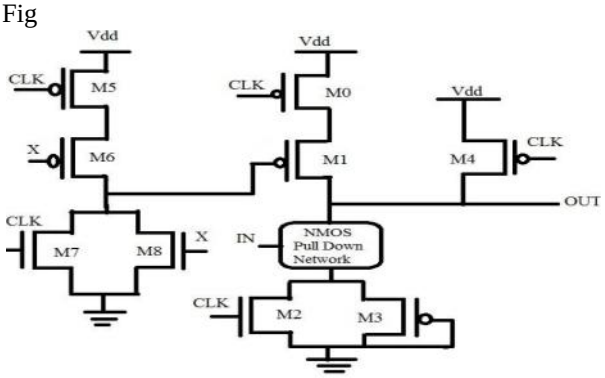

Figure 1:- Modified Constant logic style

Transistors M0 and M1 whose gates are driven by the CLK and the output of NOR gate are connected in series. This increases the resistance which in turn helps reducing the power. M4 is acting as an evaluation transistor. The NOR gate which is behaving as the self resetting logic is constituted by the transistors M5, M6, M7 and M8. M5, M6 and M7, M8 is driven by CLK and the output intermediate node X. IN values are given to the nMOS pull down network which is given according to the circuit which we have to design. Transistors M2 and M3 are connected in parallel and are placed down to the nMOS pull down network. These transistors help to reduce the power delay product. The gate of M2 is driven by the clock and M3 is at ground. Transistor M2 increases the dynamic resistance of the pull down network which successively helps to reduce the power consumption.

The circuit works under two modes of operation.

i. Pre-charge mode (CLK=0)

ii. Evaluation mode (CLK=1)

Pre-charge mode occurs when clock is low and evaluation mode happens when clock is high. When clock is low, transistor M4 gets ON and provides a high value at node X which in turn provides a low value at the output node OUT. When clock is high the transistor M2 gets ON and the nMOS pull down network is evaluated and gives the output. During this time the transistor M0 whose gate is driven by the CLK is in OFF condition. Due to this the contention mode gets wiped out in the evaluation condition

Which in turn tends for the elimination of window adjustment technique in the proposed logic? One of the reasons for the power and delay reduction in the circuit is the elimination of the window adjustment technique. During the evaluation mode the pull down network and the transistor M2 gets ON which provides high dynamic resistance which further reduces the power. Transistor M3 is in always ON condition which offers an easy discharge of the value to the ground.

CLOCKED LOGIC STYLE

The basic operation of Clocked logic style is shown in figure.

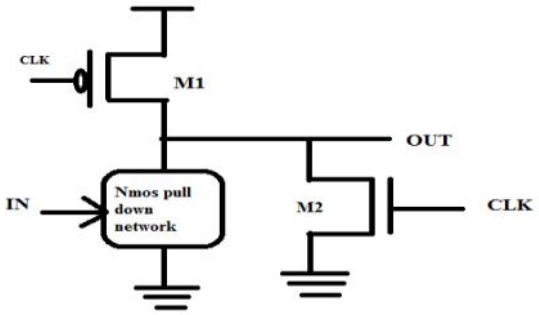

Figure 2:- Clocked logic style

The basic operation of Clocked logic is as follows: when CLK is high, the pre-discharge period begins and OUT is pulled down to GND through M2. When CLK becomes low, M1 is on, M2 is off, and the gate enters the evaluation period. If inputs (IN) are logic "1," OUT enters the contention mode where M1 and transistors in the nMOS pull-down network (PDN) are conducting current simultaneously. If PDN is off pMOS transistor. Furthermore, cascading multiple Clocked logic stages together to perform complicated logic evaluations is not practical. Consider a chain of inverters implemented in Clocked logic cascaded together and driven by the same clock, as shown in Figure 3

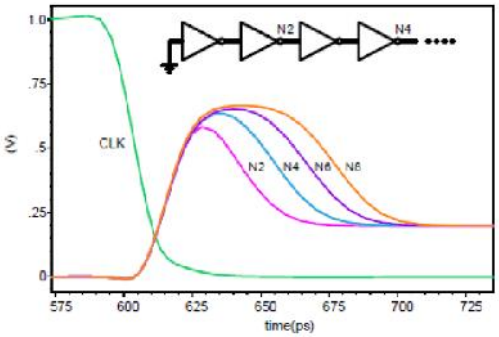

Figure 3: Simulated unwanted glitch at different logic depths in a chain of inverters implemented With Clocked logic.

When CLK is low, M1 of every stage turns on, and the output of every stage begins to rise. This will result in false logic evaluations at even numbered (i.e., 2, 4, 6, etc.,) stages since initially there is no contention between M1 and nMOS PDN because all inputs to nMOS transistors are reset to logic "0"during the reset period.

Conclusion

To overcome from the entire problem, modified constant delay logic style is proposed. It will increases higher energy efficiency, performance and reduces the delay by using the Tanner EDA software. A new high performance Modified constant delay logic style and Clocked logic style was proposed. It will increases performance and reduces the power as compared to the Constant delay logic style. Adders are designed using both existing as well as proposed logic. It is simulated in CMOS technologies for comparing performance parameter power, rise-time and fall-time. From the result it is found that MCD and Clocked logic style is having better power than the existing logic style. The Future work to this research paper can be extended by designing 8-bit, 16-bit, 32-bit adder using these logic design styles in this technology. Another scope is to extend the work to more advanced CMOS technology.

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