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Study of Power up Analysis for Switched PG Networks & Simple Switch Networks

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Abstract *– The present paper provides a detailed overview of the Power Up Analysis in Switched PG Networks and Simple Switch Networks. The Switch Characterization for Simple Switch networks and Switch Predictions are also studied and validated with the help of results and observations. The reason for limiting the use of 'Sleep Transistor 'technique and prominent use of Power Up Analysis are also mentioned in the paper. SPICE simulation is used to validate the results.*

Keywords*: PG Networks, Power Up Analysis, Simple Switch Networks, Sleep Transistor, SPICE.*

I. Introduction

One of the popular techniques to reduce leakage is to use gated power supply [1, 2, 3]. Shekhar [1] has highlighted a technique called 'sleep transistor' and challenges associated with that. This technique proposes to gate power supply using a high threshold transistor when not required. The 'sleep transistor' also known as 'power switch' turns off power supply when a portion of chip is idle and thus saving leakage current. Apart from design challenges, the technique has additional Design Analysis challenges as mentioned below:

1. When Power Supply turns on from off state, a huge capacitive load gets charged causing a huge surge in current causing Power Supply Noise (PSN). This can couple with signal lines causing state change or delay change. It can also remain within supply network but causing huge dynamic IR drop that in turn affects circuit performance. The goal is to predict the surge and control that.
2. The Transistor in series with the supply acts as huge resistor in normal mode of operation causing additional IR Drop. This in turn degrades the performance. The IR Drop across the transistor can be as high as 5-20mV. The goal is to do an average IR drop analysis to access the impact of switch.
3. Optimization of switches to get the best leakage improvement. The optimization has area penalty or IR drop or Power Supply Noise as cost parameters. For example, low number of switches gives good leakage improvement but high IR drop and Power supply noise.
4. When power supply goes down, all sequential logic in the virtual power domain losses its state. This puts extra constraint overall on system behavior. There is also a technique where the state is preserved through 'retention flops'. [4,5] The technique does need extra power routing to save state as well as control logic. The timing analysis needs to capture the mode switching.
5. Placement and Routing of extra signals, special cells (like retention flops etc) and virtual power network.
6. Leakage and number of power switch trade off.
7. Power routing closes immediately after floor plan. The switches need to be placed by this time. It is important to have early power up analysis flow to compute required number of optimal switches meeting the peak current surge as well as IR drop and leakage needs.

Often, PSN is non-negotiable parameter and design-planning goal is to identify total number of switches that limits PSN to user-defined level. This paper describes an analytical method to determine optimum number of power switches and power up glitch. Section

II elaborates on switched PG network and PSN problem. Section III outlines the approach to analyze such networks. Section IV correlates the results we have achieved with SPICE and the efficiency of algorithm.

II. Switched PG Networks

Power Supply Noise is widely acknowledged research domain in today's high performance designs. There is various analysis techniques also proposed in literature. [6-11] However, there is not much awareness on Power Supply Noise caused by turning on the power domains when gated power supply is used. Figure 1 shows switch network for 1M-gate design and Figure 1.1 shows a current glitch and voltage ramp on an arbitrary switch output. Note that the current surge can remain for a considerable amount of time causing performance impact to 'on' blocks.

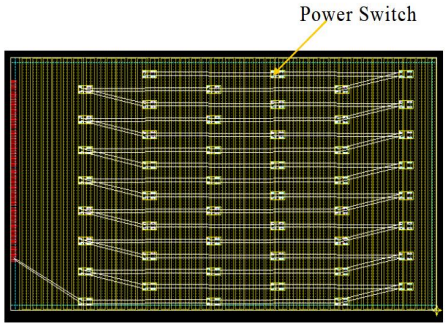

Fig.1. Layout of 1M Gate with switch Network

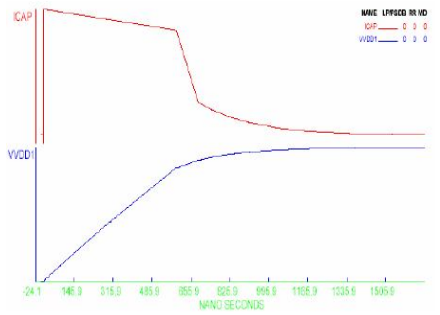

Fig .1(a) Current Glitch and Voltage Ramp at Arbitrary Switch Output.

A typical PG network with Power Switches can be represented as shown in Figure 2. Some of the characteristics of this network are: [12]

- 2 domains – one golden domain and non-gated power supply, second multiple virtual domains and switched power supply.
- All virtual domains are unconnected within. They are connected to golden domain through switch network.
- Switch network consists of one or more different kind of switches for a given domain.
- Switch network across virtual power domains are not shared.
- Random logic is connected to golden domain as well as all virtual domains.
- Control logic enables any one or more virtual domains to turn on/off any time.
- Further, any switch network consists of parallel network or sequential network or combination of both. Parallel configuration allows all switches to turn on Simultaneously whereas sequential configuration allows each switch to turn on one by one after some delay.

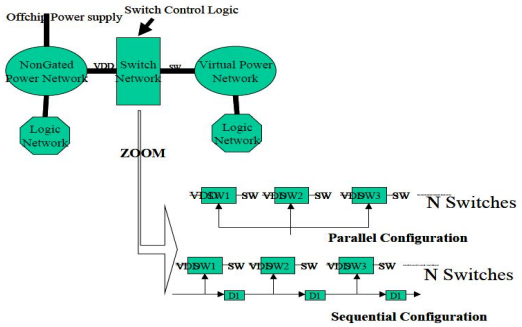

Fig .2. Typical PG Network With Power Switches

When the power supply is 'off' and virtual network is disconnected, the current that passes through is leakage current. If leakage current of the virtual logic is significantly higher than that of switch network leakage, leakage current improvement happens. When the switches are turned on i.e. when the power supply connects to virtual power network, the loads in virtual power network start getting charged. Loads include interconnect capacitances, gate capacitances as well as the circuit diffusion/diode caps. The amount of current being sunk by these caps depends on the ability of switch network to provide charge in a given time. Due to fast current need of the virtual power domain, there is L*di/dt noise being injected into circuit that can affect normal functioning of the golden power domain. Note that despite of capacitive load dominating, the peak current is still limited by saturation current of switch causing current profile we got in Figure 5.3.

II.1 Switch Network Analysis

Switch Network Analysis (SNA) early in design-planning includes decision of switch network topology, identification of switches to be used, total system timings for turning on/off power domains as well as total power supply noise contribution by a switch network. Sequential configuration allows configuring delay such that the peak current at any point of time can be controlled to meet the specification of system noise and hence the tradeoff between the total time systems requires to on/off virtual network and the noise criteria.

This information should go to the placement and routing tools for physical design. Further, switch network contribution comes from maximum current surge it causes and the point of optimization there is total number of switches of each type in the network and delay. Following assumptions are made to keep the analysis simple but in reality the solution can be extended to handle them.

- Delay between two consecutive switches is same.
- 2 types of switches exist in the network.
- Voltage at any node in virtual power network is of the same value at any time instant during power ON if there is zero static IR drop.
- Switch Network is sequential. Parallel configuration essentially means a BIG switch - all transistors forming a BIG switch with characteristic lumped to a single MOS.

High-level flow for the analysis is shown in block diagram Fig. 3.

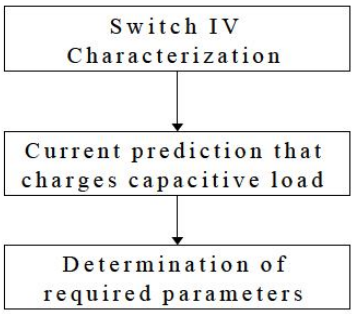

Fig .3. Schematic Switch Analysis Flow

II.2 Switch Characterization

Switch IV Characterization includes current being sourced through switch for different voltages between golden and virtual power port of switch. This is achieved using transient SPICE simulation of the switch. The data is stored in value-pair (voltage-current) format for further Processing. Switch characterization also involves switch ON resistance measurement. This is resistance thatswitches offer during normal functionality i.e. when switches are turned ON and virtual power network is connected to golden power network. This is measured by putting 10mV battery across switch and measuring current. This resistance value is later used for average IR drop analysis across switch.

III. Current or Switch Prediction

Current prediction is done based on simplified extracted model of block under consideration as Figure 4. The switch network is modeled along with its detailed connectivity and timing whereas the logic connected to virtual domain is modeled as capacitive load. Current through switch is predicted in infinitesimal small time duration. The CV characteristic is applied here as below:

Current(I) =dq/dt OR dq = I dt ……1

But dq = C * dv ……2

Hence dv = I * dt / C ……3

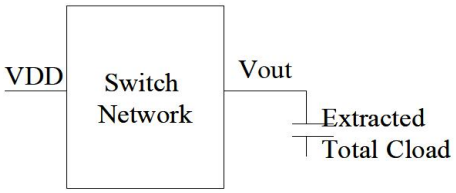

Fig .4. Analysis Model of Virtual Power Network

Equation 3 forms the basis of Algorithm 1 described in next section. The delay between two consecutive switches is used to predict the charge being supplied by the switch to virtual power network domain. The IV table of the switch is used to predict current by further dividing delay into infinitesimal small time duration as shown in Figure 4.1. Based on the initial voltage and Charge supplied, the voltage has been derived when the next switch just starts turning on. This process continues till either all switches are turned on or the specified voltage level is reached. Further, the same method continues if all the switches are turned on but voltage value is lower than the ideal voltage value (VDD golden) to predict the maximum surge in current. Predicted number of switches is used to predict static IR drop across switch network as explained in Algorithm 2.

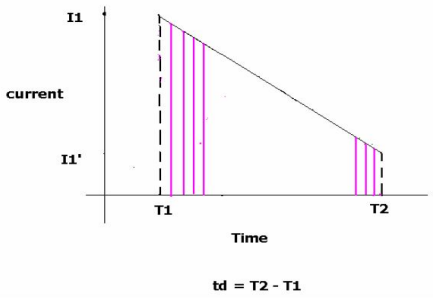

Fig.4(a)Infinitesimal Time Division for current Prediction

Parameters those can be analyzed through this setup include:

- Total number of switches required reaching a required voltage value.
- Alternatively, voltage value that can be reached with given number of switches.
- Maximum current surge that will happen given the number of switches.
- Delay impact of consecutive switches while they turned on.
- IR drop across switch network

III.1 Algorithm for Power Switch Network Analysis

Initialize load voltage to zero and current charging to Zero.
{
For each, infinitesimal small times period, predict the current based on the voltage at lumped load from IV table of the switch type.
Identify the actual current based on the number of switches turned on at the particular instance of time.
Track the current at VDD i.e. if the new current is greater than old one; assign maximum surge current to new current.
Calculate the rise in voltage in the infinitesimal small time based on equation (3).
Continue till either all the switches are turned on or the desired voltage level is reached.
}
Print maximum surge current and voltage level reached after turning on some specific switches as required by user.

III.1.2. Algorithm for Static IR Drop analysis across Power Switches

{
Read switch characterization data – for static IR drop, read ON Channel resistance (RON)
Determine total number of switches required to reach desired voltage level – desired voltage level is specified by user – by "Algorithm for power Switch Network Analysis"
Effective resistance of the switches predicted above (N) is: RON/N
Compute power consumption of switched off or virtual power network using any methods described in this work (can be outside this work also!)
Compute average current consumption of the virtual power network. Iavg = Pavg/VDD
Static IR drop across switch network is: Iavg*RON/N.
}

IV. Conclusion

Traditional approach to study above would be full-fledged SPICE simulation that includes virtual power network and switch network where each switch is turned on after some delay.
Alternately we can reduce the virtual power network by modeling the interconnect load and gate capacitance with a huge distributed capacitance and on channel transistor resistance with effective resistance in series with each distributed C to reduce the number of active elements and simulate the reduced power network using SPICE (Figure 5). This approach gives orders of improvement in terms of simulation time but the run time is still days.

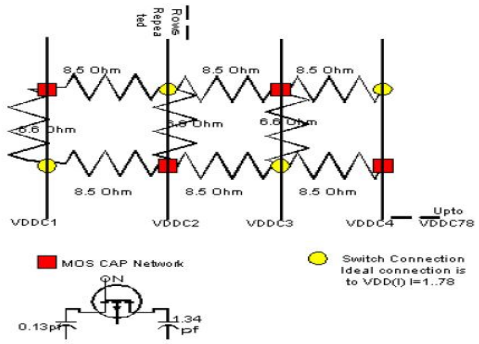

Fig .5.Reduced Switched Network for Validation

The technique we presented here is static in nature and reduces the runtime to few minutes and gives very good correlation to techniques described above. The algorithms described above were analyzed with switches designed in TI's 90 nm node. All the results below are for a 1M equivalent gate block. 1M Gates could not be simulated using SPICE along with switches so a simplified model described in previous paragraph was employed to get SPICE accuracy data while keeping switch network intact. We had employed switch network with two kinds of switches for this analysis [12]. One set of switches took the virtual domain till a specific voltage level and second kind of switches with high capacity were turned on in a sequential manner to measure surge in current.

Table I shows prediction of switches for given voltage. When the numbers of switches are increasing the algorithm gives results within 1% accuracy to SPICE based simulation whereas when the numbers of switches are less, the inaccuracy is within 10%. In other words, the actual number is quite close to realistic number with accuracy 1-10%. This table also shows the current surge prediction and the switch number which turns ON causing maximum peak. Essentially, along with surge, we predict the switch at which the maximum surge occurs. This helps to further optimize the 2nd type of switch network. Table II shows voltage prediction given the number of switches.

The advantage of whole solution comes from the superlative run time improvement that enables early analysis and tradeoffs in the design – Table III. The runtime clearly outweighs the small inaccuracy in switch prediction or voltage prediction. Note that runtime does not include switch IV characterization time since it is one time effort. In static analysis, we can dump lot more information quickly as per the need to understand certain behavior for tradeoff analysis. We can also predict time domain behavior of voltage and current using the approach described in this work. Figure 6.1 compares predicted voltage over time to few arbitrary nodes simulated in SPICE. Figure 6 compares predicted current over time to current measured at VDD. This is good

considering that the analysis is targeted for early trade off analysis.

TABLE I

Vdesired (mV)	Actual #Switches	Switches by Algorithm	Current Surge (mA)	Current Surge after #switches
20	380	403	950	123
69	760	771	881	114
271	1560	1554	749	100
583	2340	2328	467	97
869	2964	2971	266	81
1170	4368	4308	24	43

SWITCH PREDICTION BY PROPOSED ALGORITHM

TABLE II

# Switches	Simulated Voltage (mV)	Voltage by Algorithm	Surge Current	Surge Current after switch # (mA)	%Error in voltages
780	63	70.54	892	101	11
1560	280	273.53	784	94	-0.2
2340	587	589.26	546	78	0.38
3120	926	927.7	263	64	0.18

VOLTAGE PREDICTION

TABLE III

No. of switches	Simulation Time (in days)	Algorithm Runtime (in mts)
780	~1.5	< 1
1560	~4	< 1
2340	~5	< 1
2940	~6	< 1

POWER UP ANALYSIS- RUNTIME COMPARISION

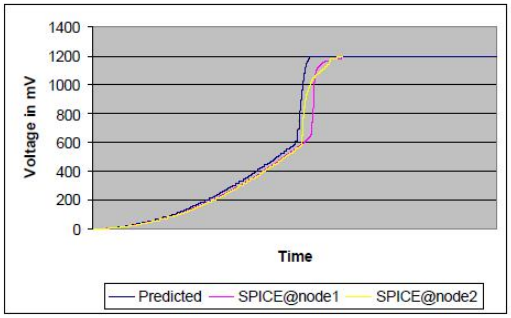

Fig .6. Current Comparison over Time

There are various techniques to improve leakage power of the design - 'gated power supply' or 'sleep transistor' or 'switched power network' is one of the efficient methods to reduce the leakage power. The analysis techniques described in this work helps in giving quick data for architecture level decisions while using 'switched network' technique. The runtime is in few Seconds and hence Design Team can do lots of iterations to get the optimum number of switches. The analytical method to calculate total no of switches is fast since it involves one time SPICE simulation – only IV characteristic of switch - and rest of the analysis is performed using static analysis. We have also analyzed 'power on glitch' for the design using the method that contributes to Power Supply Noise during power up. All the results are closely matching with SPICE simulation.

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