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Design and Analysis of various Phase Locked Loop (PLL)

Rachit Kumar Kourav[1], Braj Bihari Soni [2]
[1]*M.Tech Research Scholar, ECE NIIST RGPV, rachitkourav@gmail.com, India;*
[2] *Assistant Professor, ECE NIIST RGPV, brizsoni@gmail.com, India;*

Abstract *– This paper heresy an assortment of available Phase Locked Loop architectures. A PLL system having various types of phase detector, charge pump, loop filter, voltage controlled oscillator are existing in this paper. The troubles linked with the linear PLL are also discussed .A variety of models of PLLs which are Linear PLL, Digital PLLs, and All digital PLLs are implemented and simulate the results of implementation on MATLAB Simulink which gives the improved presentation of all PLLs.*

Keywords*: PLL, Phase Detector, Charge Pump, Loop Filter, Voltage controlled oscillator, Linear PLL.*

I. Introduction

Phase locked loops have been presented in literature ever since 1923 [1]. It was only in late 1970s that PLLs were used in modern communication systems due to the rapid development of integrated circuits. Since then the use of PLLs has been shifted from high precision instruments to more reliable consumer electronic products. A PLL is a circuit synchronizing an output signal (generated by an oscillator) with a reference or input signal in frequency as well as in phase. In the synchronized (locked) state, the phase error between the oscillator's output signal and the reference signal is zero, or it remains constant [2].

Widespread use of PLL began with TV receivers during 1940s. PLLs were used to synchronize the horizontal and vertical sweep oscillators to the synchronous pulses [3]. PLLs have wide applications such as frequency selective demodulation, signal conditioning, reference signal source, grid utility [3], [4]. From luxury items to indispensable tools, wireless systems have quickly penetrated into all aspects of our lives. All these devices have common requirements of a preferred monolithic implementation, low power, reduced physical size and high accuracy [5], [6]. From early 1970's, strong interest in the implementation and design of digital PLLs (DPLL) started because of the popularity of large scale integrators (LSIs) [7]. Aside from the obvious advantages associated with digital systems, a digital version of PLL alleviates some of the problems associated with its analog counterpart; namely:

1. Sensitivity to dc drift and component saturation.
2. Difficulty in building higher order loops.
3. Need for initial calibration. [8]

In addition, with the ability to perform sophisticated signal processing on the IC chips, DPLL's are more flexible and versatile than analog PLL's [7]. The DPLL is still a semi analog circuit and is referred to as hybrid PLL. The all digital PLL (ADPLL) and software PLL has recently gained increased attention. The ADPLL is built entirely from logic circuits and has replaced the classical DPLL in many applications, especially digital communications [7].

Phase locked loops (PLLs) are extensively used in microprocessors and digital signal processors for clock generation and as a frequency synthesizers in RF communication systems for clock extraction and generation of a low phase noise local oscillator [9].

II. Necessary Concept of PLL

A PLL is a device which locks an output signal phase relative to an input reference signal phase .The signals of interest may be any periodic waveform but are typically sinusoidal or digital clock [10]. PLL's are typically divided into broad categories listed in Table 1 as per [6] terminology.

Table 1. General PLL category

S No.	PLL	Phase Detector	Loop Filter	Oscillator
1	Linear PLL (Analog PLL)	Analog	Analog	Voltage Controlled Oscillator (VCO)
2	Digital PLL (DPLL)	Digital	Analog	Voltage Controlled Oscillator (VCO)
3	All Digital PLL (ADPLL)	Digital	Digital	Digitally Controlled Oscillator (DCO)

4	Software PLL (SPLL)	Software	Software	Software

After the invention of PLL in1932, the basic phase locked loop has remained nearly the same but its implementation in different technologies is still a challenge for engineers.
A PLL is a feedback system that compares the output phase with the input phase. The comparison is performed by the phase compensator or phase detector. A phase detector is circuit whose average output voltage is proportional to the phase difference between two inputs. While in ideal case relation between output voltage and phase difference is linear.

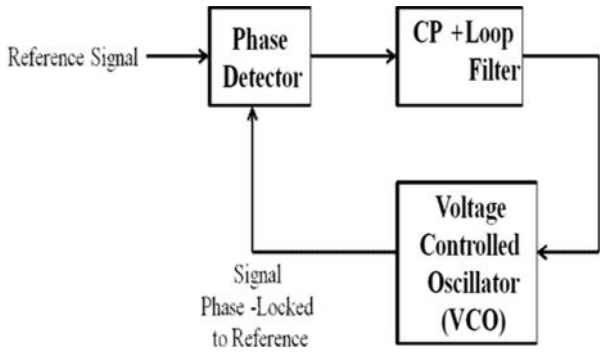


Fig 1: Block Diagram of Basic PLL

This output voltage passes through the LF and then as an input to the VCO to control the output frequency. Due to this self-correcting technique, the output signal will be in phase with the reference signal. When both signals are synchronized, the PLL is said to be in lock condition. PLL make the phase error between the two signals to be zero at this time [11]. If the difference between the input signal and the VCO is not too big, the PLL eventually locks onto the input signal. This period of frequency acquisition, is referred as pull-in time, this can be very long or very short, depending on the bandwidth of the PLL. The bandwidth of a PLL depends on the characteristics of the PD, VCO, and on the LF [12].

III. PLL Components

III.1 Phase Detector

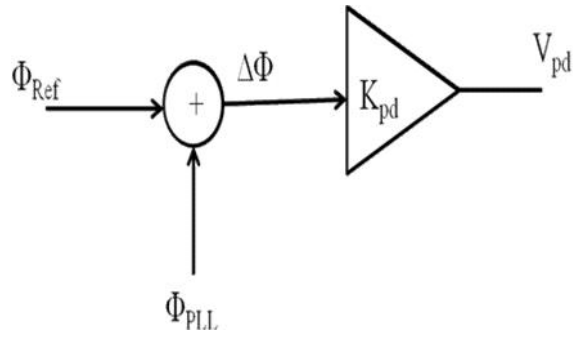


Fig 2: Simplified model of a Phase Detector

The role of a PD in a PLL circuit is to provide an error signal, which is some function of the phase error between the input signal and the VCO output signal. Let $\Delta\Phi$ represents the phase difference between the input phase and the VCO phase. In response to this phase difference the PD produces a proportional voltage V_{pd}.

$$\Delta\Phi = \Phi_{Ref} - \Phi_{PLL} \qquad (1)$$

The phase detector converts the input phase difference $\Delta\Phi$ to an output signal Vpd with a gain factor Kpd.

$$V_{pd} = K_{pd} \cdot \Delta\Phi \qquad (2)$$

The phase detector can be classified based on different applications and implementations.
They are two types of phase detectors, namely sinusoidal phase detectors and square signal phase detectors. A sinusoidal phase detector has a phase detection interval (- π/2 to + π/2). It operates as a multiplier, which is a zero memory device. The square signal phase detector, also called as sequential phase detector are implemented using sequential logic circuits. They are usually built from digital circuits and operate with binary rectangular input waveform. Accordingly they are called as digital phase detector [13].

The different phase detectors are classified in Table 2 as per [14-15].

Table 2. Class and linear range of phase detectors

Type	Class	PD Gain (K_{pd})	Linear Range	Applications
Mutiplier	Analog	Non linear and proportional to the amplitude of the input signal	-π/2 to + π/2	Frequency modulation and demodulation
XOR	Digital	(Vh- V1)/π	-π/2 to + π/2	Data and clock recovery
RS latch	Digital	(Vh-Vl)/2 π	-π to + π	Deskewing
PFD (Phase frequency Detector)	Digital	Vh-Vl)/4 π	-2π to + 2π	Clock synchronization and frequency synthesis

***III.2** Loop Filter*

The filtering operation of the error voltage (coming out from the PD) is performed by the loop filter (LF). The output of PD consists of a dc component superimposed with an ac component. The ac part is undesired as an input to the VCO; hence a low pass filter is used to filter out the ac component. LF is one of the most important functional blocks in determining the performance of the loop. A LF introduces poles to the PLL transfer function, which in turn is a parameter in determining the bandwidth of the PLL. Since higher order loop filters offer better noise cancellation, a loop filter of order 2 or more are used in most of the critical application and PLL circuits especially in RF communication systems [16].

The Transfer function of second order loop filter is given by

$$F(S) = \frac{V_{CTRL}(S)}{I_{CP}(S)} = R + \frac{1}{C_1 S} \| \frac{1}{C_2 S} \qquad (3)$$

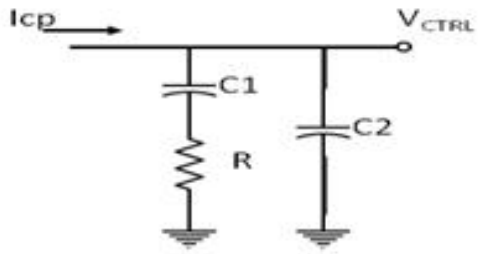


Fig 3: Second Order Loop Filter

where VCTRL is the voltage across the loop filter and I_{CP} is the current coming from the charge pump circuit

After simplification of equation (8), we get

$$\frac{R C_1 S+1}{RC_1C_2 S^2+ S(C_1+C_2)} = K_P.\frac{S+\omega_z}{S.\left(\frac{S}{\omega_p}+1\right)} \qquad (4)$$

Where $K_F = \frac{RC_1}{C_1+C_2}$

Thus, we have obviously acquire a zero ω_z and a pole ω_p which are given by

$$\omega_z = \frac{1}{R C_1} \qquad (5)$$

$$\omega_p = \frac{C_1+C_2}{C_1 C_2 R} \qquad (6)$$

III.3 Charge Pump

The charge pump current drives the PFD output. It converts the output digital PFD signal into analog signal. Basically, the charge pump consists of a current source, a current sink and two switches. However, the charge pump is usually followed by a passive loop filter that integrates the charge pump output current to a VCO control voltage. Thus, the charge pump output voltage is always equal to the VCO control voltage. The charge pump either sources or sinks current according to UP and DOWN signal. This amount of current is converted into controlled voltage by the loop filter for tuning the VCO [3]. To avoid current mismatching, the source and sink current values should be same. If the source and sink current of the charge pump are both I_{CP} the phase detector gain is given by

$$K_d = \frac{I_{CP}}{2\pi} \qquad (7)$$

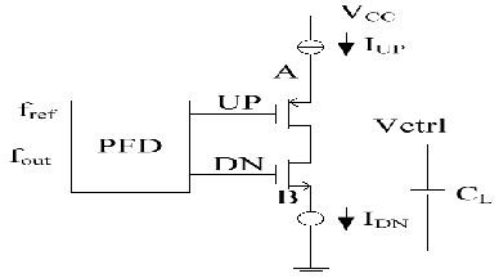


Fig 3: Basic Charge Pump Circuit

The control voltage increases when the reference signal leads the feedback signal and decreases when reference signal lags the feedback signal.

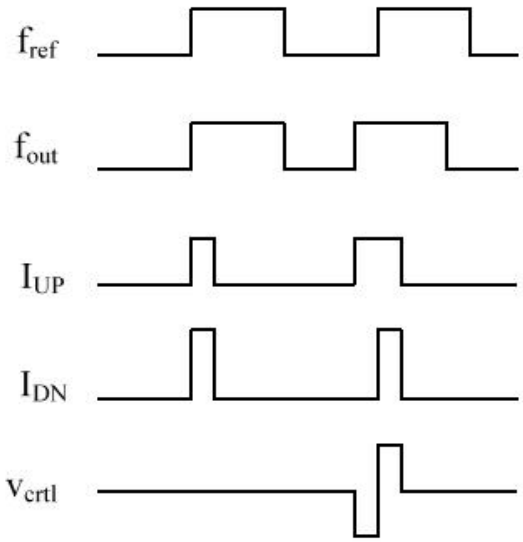


Fig 3: Charge and Discharge Mismatch

III.4 Voltage Control Oscillator

is the most impotent building block of the PLL which generates the required clock signal with a controlled frequency. Oscillator can be classified based on the control signal applied as:
1. Voltage controlled oscillator (VCO): The control signal applied is a voltage signal.
2. Current controlled oscillator (ICO): The control signal applied is a current signal.
3. Digital controlled oscillator (DCO): The control signal applied is a digital word.

If the frequency is a linear function of the control voltage Vinvco, the VCO frequency

$$f_{out} = f_o + K_v V_{inVCO} \qquad (8)$$

Where f_o is the free running frequency and K_v is the VCO sensitivity

The main constraints for the VCO are:
1. Phase stability
2. Large frequency deviation
3. High VCO sensitivity
4. Linearity of frequency versus control voltage
5. Capability of accepting wide band modulation [13].

Four types of VCO commonly used are:
1. Voltage controlled crystal oscillator
2. Resonator oscillator
3. RC multivibrators
4. Ring oscillator [3]

The phase stability can be enhanced by a number of ways:
1. Using high Q crystal and circuit
2. Maintaining low noise in the amplifier portion.
3. Stabilizing temperature, and

4. Keeping mechanical stability. [13]

Digitally controlled oscillator is basically a programmable divide by N circuit. The output of a stable oscillator drives the counter which increases by one every clock cycle. The content of the counter is compared with the input and when they are matched, the comparator sends an output pulse which is the DCO output and resets the counter. By varying the control input N, DCO period can be controlled. [8]

IV. Literature Survey

Table 3. Literature Review

Title	A 1-GHz Charge Pump PLL Frequency Synthesizer for IEEE 1394b PHY	High Current Matching over Full-Swing and Low-Glitch Charge Pump Circuit for PLLs	CMOS Charge Pump With No Reversion Loss and Enhanced Drivability	Dynamic Self-Regulated Charge Pump With Improved Immunity to PVT Variations	An Ultra-low Power Charge-Pump PLL with High Temperature Stability in 130 nm CMOS
Publications	Journal Of Electronic Science And Technology, Vol. 10, No. 4	Radio engineering, Vol. 22, No. 1	IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 6,	IEEE Transactions On Very Large Scale Integration (VLSI) Systems, Vol. 22, No. 8	
Year	December 2012	APRIL 2013	June 2014	August 2014	2015
Author	Jin-Yue Ji, Hai-Qi Liu, and Qiang Li	De-zhi WANG, Ke-feng ZHANG, Xue-cheng ZOU	Joung-Yeal Kim, Su-Jin Park, Kee-Won Kwon, Bai-Sun Kong, Joo-Sun Choi, and Young-Hyun Jun	Sleiman Bou-Sleiman, Member, IEEE, and Mohammed Ismail, Fellow, IEEE	Anh Chu, Navneeta Deo, Waqas Ahmad, Markus Törmänen and Henrik Sjöland
Technology	0.13 µm	0.18 µm	46nm	90nm	130nm
Supply Voltage	1.2V	1.8V	1.96V	1.32V	1.2V
Current Consumption	1.6mA	40 µA	0.4mA	450 µA	77 µA

V. Simulation of PLL in Simulink

V.1 Linear Phase Locked Loop

Linear PLL uses a mixer as a phase detector; the output of the mixer is a dc component that is proportional to the phase difference and a component at a frequency that is twice the input frequency. A low pass Butterworth filter is used as a loop filter to get rid of the second component. The output of the loop filter is fed to a VCO that increases the frequency if there is a positive phase difference and then decreases the frequency if there is a negative phase difference [6].

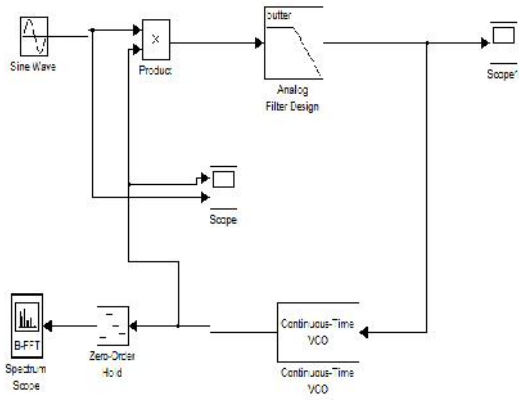


Fig 5: Linear Phase Lock Loop in Simulink

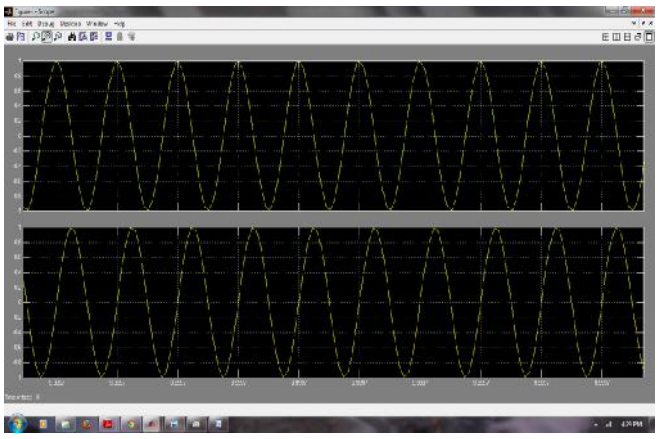


Fig 6: Output Wave form of Liner PLL

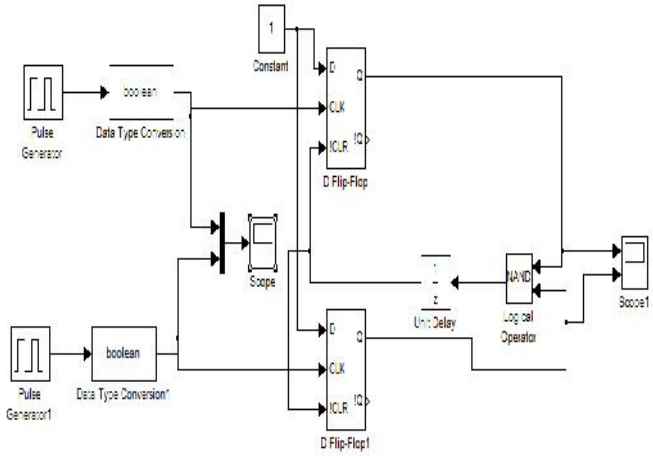
It is strongly encouraged that the authors may use SI (International System of Units) units only.

V.2 Digital Phase Locked Loop

Digital PLL uses a phase frequency detector as depicted in figure 3.3. The PFD is built using two D flip flops whose output is denoted by U and D respectively. The PFD can be in one of the four states

1. U = 1, D = 1
2. U = 1, D = 0
3. U = 0, D = 1
4. U = 0, D = 0

Whenever both the flip flops are in a high state, the AND gate will reset both the flip flops, hence the device acts as a tristable device. If PFD generates U signal, the VCO speed up. On the contrary, if a D signal is generated, VCO slows down [17].



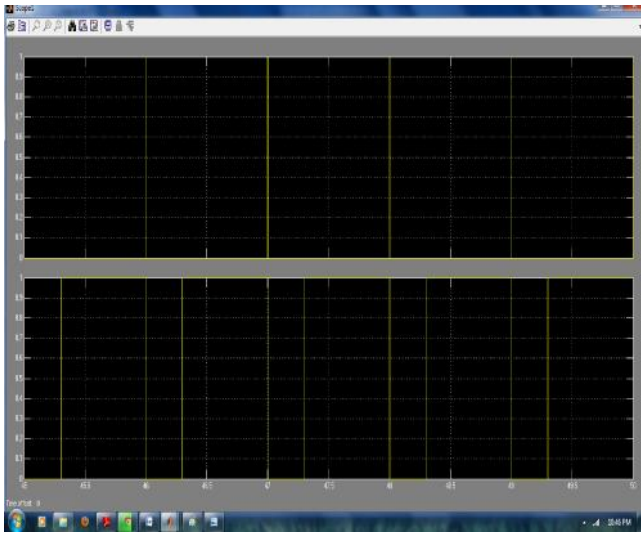


Fig 7: PFD of Digital Phase Locked Loop

Fig 8: Output Wave form of PFD of DPLL

Better results can be achieved with a charge pump and a loop filter. The charge pump, "pumps" current into a 2nd order loop filter. The branch voltage of the loop filter is used as input to the VCO. A digital phase frequency detector (PFD) determines whether a positive or negative current is pumped into the filter. Phase lead corresponds to a negative frequency (output and thus VCO frequency decreases) whereas phase lag corresponds to a positive current.

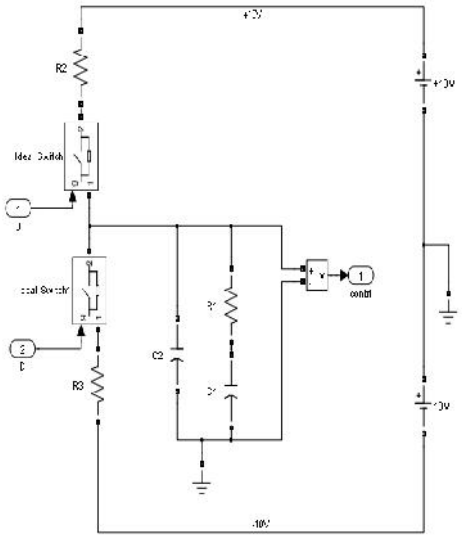


Fig 9: Charge pump of DPLL

V.3 All Digital Phase Locked Loop

PLL are used more in the digital domain, hence apart from the phase frequency detector, the loop filter and VCO also needs to be converted to digital time systems. Digital filter is used as a low pass loop filter. The VCO is rep laced by an NCO (numerically controlled oscillator).

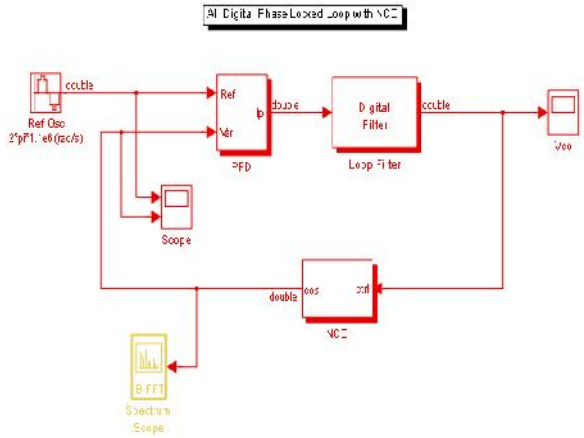


Fig 10: All Digital PLL in Simulink

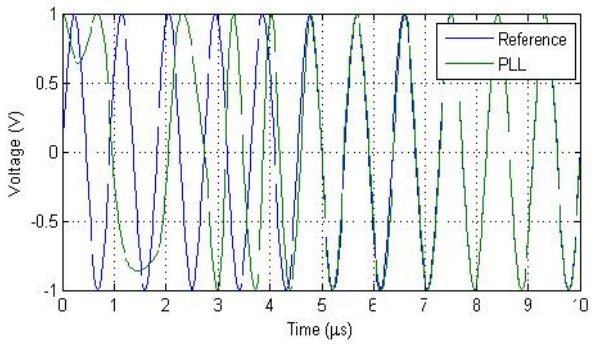


Fig 11: Output of AD PLL

VI. Conclusion

This paper reviews the PLL technique which is applicable to communication and servo control system. A summary of PLL technology and its development trends are included. It is pointed out that the development of better PLL technology is continuing.

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